Exhibit A

United States Patent [19]

Babin

[11] **Patent Number: 4,951,005**

[45] **Date of Patent: Aug. 21, 1990**

[54] **PHASE LOCKED LOOP WITH REDUCED FREQUENCY/PHASE LOCK TIME**

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[21] Appl. No.: **457,465**

[22] Filed: **Dec. 27, 1989**

[51] **Int. Cl.**[5] **H03L 7/18**

[52] **U.S. Cl.** ..... **331/16**; 331/1 A; 331/25

[58] **Field of Search** ..... 331/1 A, 16, 18, 25, 331/27; 455/260

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,378,509	3/1983	Hatchett et al.	331/1 A X
4,714,899	12/1987	Kurtzman et al.	331/1 A

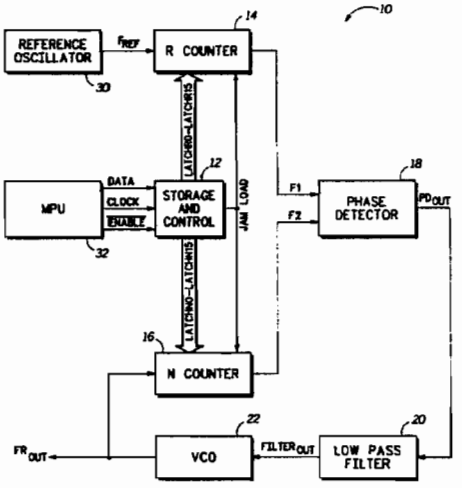
Primary Examiner—David Mis

Attorney, Agent, or Firm—Robert L. King; Paul J. Polansky

[57] **ABSTRACT**

A phase locked loop for providing a programmable frequency output signal with reduced phase-frequency lock time. A phase detector detects a phase difference between a reference frequency divided by a first number, and a frequency of the output signal divided by a second number. First and second counters receive the first and the second input numbers to divide a respective frequency. Whenever an input number is loaded, a load signal resets the phase detector and causes each counter to be loaded, which reduces the lock time of the loop.

10 Claims, 2 Drawing Sheets



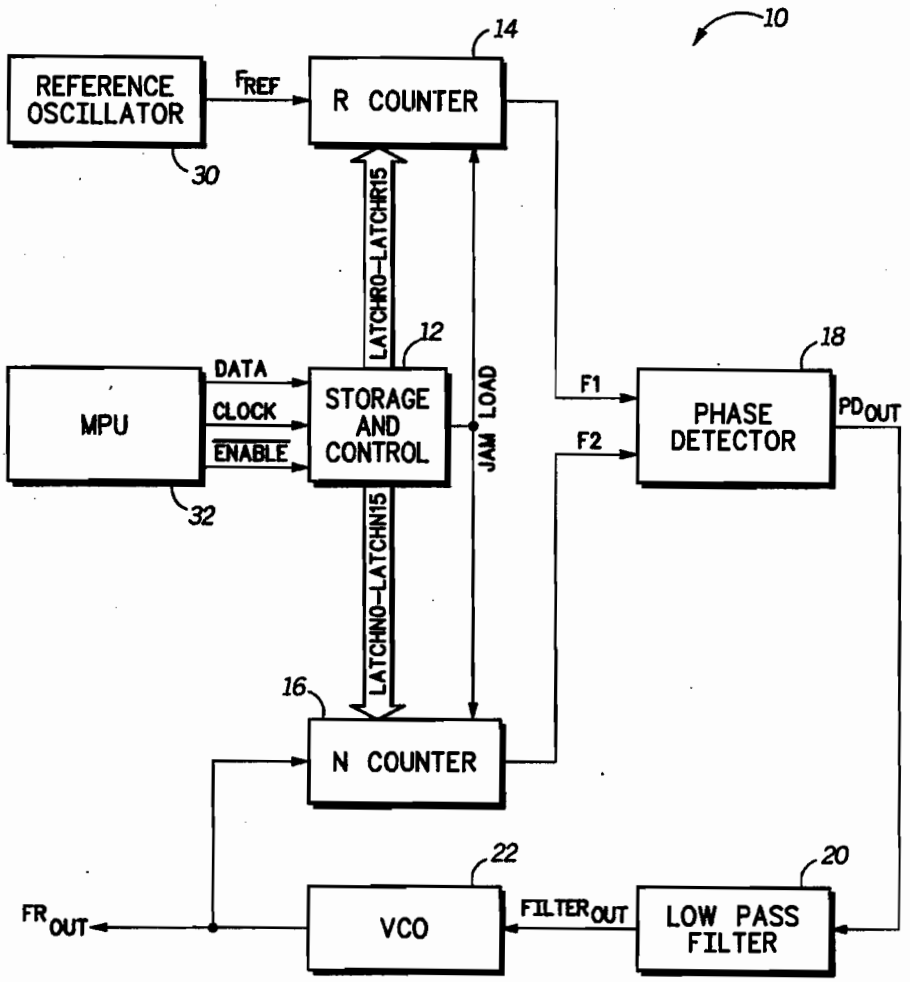

10
14
REFERENCE OSCILLATOR
FREF
R COUNTER
30
LATCHR0–LATCHR15
12
18
DATA
CLOCK
ENABLE
MPU
STORAGE AND CONTROL
JAM LOAD
F1
F2
PHASE DETECTOR
PDOUT
32
LATCHN0–LATCHN15
16
N COUNTER
22
20
FROUT
VCO
FILTEROUT
LOW PASS FILTER

FIG. 1

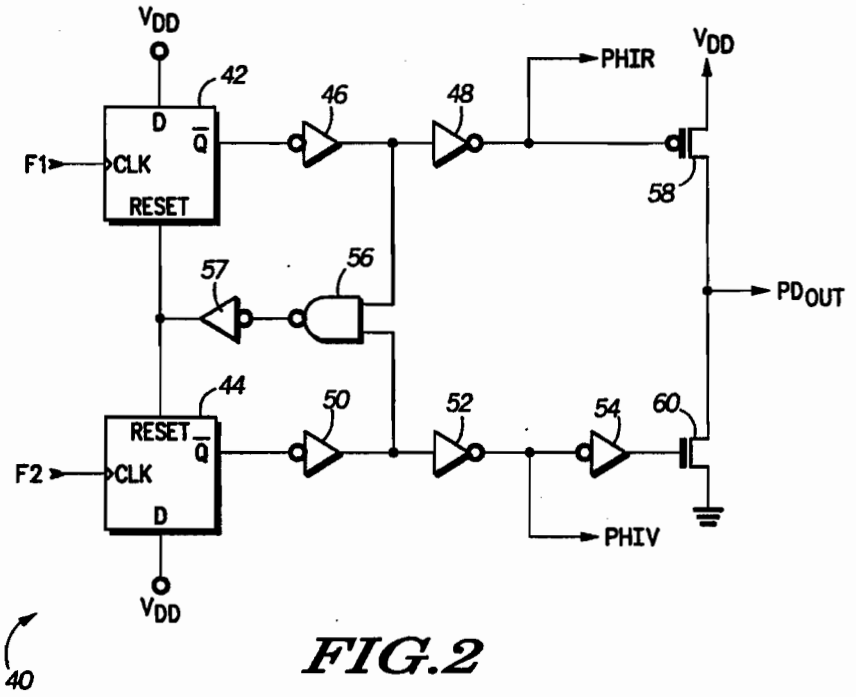

VDD
42
D
Q
F1
CLK
RESET
46
48
PHIR
VDD
58
57
56
PDOUT
44
RESET
Q
50
52
54
60
F2
CLK
D
PHIV
VDD
40

FIG.2

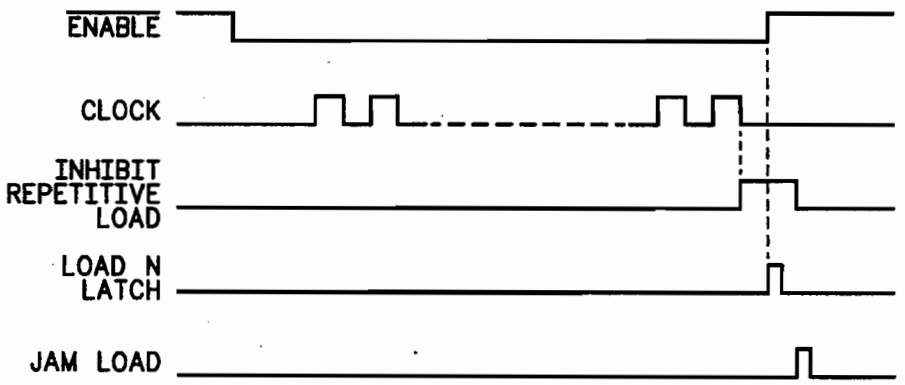

ENABLE
CLOCK
INHIBIT REPETITIVE LOAD
LOAD N LATCH
JAM LOAD

FIG.3

PHASE LOCKED LOOP WITH REDUCED FREQUENCY/PHASE LOCK TIME

FIELD OF THE INVENTION

This invention relates generally to phase locked loops, and more particularly, to programmable, digital phase locked loops used for frequency synthesizers.

BACKGROUND OF THE INVENTION

Phase locked loops (PLLs) have important uses in communications applications. A PLL frequency synthesizer, one such use, generates an output signal having a programmable frequency to be used in tuning of two or more communication channels. Typically, a microprocessor programs the frequency of the output signal. In many applications, the programmed frequency must change dynamically. For example, the frequency normally generated by the PLL frequency synthesizer is used to tune a communications signal, but periodically the frequency must be changed to tune an auxiliary channel. The functioning of the phase locked loop may be enhanced by using a digital phase detector to measure a phase difference between the output signal and a proportion of a reference signal, and to adjust the output signal in response to a detected phase difference. Performance of PLL frequency synthesizers using digital phase detectors must continually be improved to meet increased performance requirements of communication circuits.

BRIEF DESCRIPTION OF THE INVENTION

Accordingly, it is an object of the present invention to provide a phase locked loop with improved lock time.

It is another object of the present invention to provide a phase locked loop with an improved phase detection mechanism.

In carrying out these and other objects of the invention, there is provided, in one form, a phase locked loop comprising an input portion, a reference portion, a phase detection portion, and a loop portion. The input portion stores a first and a second predetermined number in response to a plurality of input signals. The reference portion is coupled to the input portion, and provides a first signal in response to the first predetermined number of cycles of a reference signal, a second signal in response to the second predetermined number of cycles of an output signal, and both the first signal and the second signal in response to the input portion storing either the first predetermined number or the second predetermined number. The phase detection portion is coupled to the reference portion, and provides a phase difference signal in response to a difference in logic state between the first signal and the second signal. The loop portion is coupled to the phase detection portion and to the reference portion, and provides the output signal as a frequency proportional to the phase difference signal.

These and other objects, features and advantages will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates in block diagram form a phase locked loop in accordance with a preferred embodiment of the present invention;

FIG. 2 shows a schematic of a phase detector used in the phase locked loop of FIG. 1; and

FIG. 3 shows a timing diagram useful in understanding the phase locked loop of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates in block diagram form a phase locked loop 10 in accordance with a preferred embodiment of the present invention. Phase locked loop 10 comprises a storage and control portion 12, an R counter 14, an N counter 16, a phase detector 18, a low pass filter 20, and a voltage controlled oscillator (VCO) 22. Also shown are a reference oscillator 30, and a microprocessor (MPU) 32, which are not a part of phase locked loop 10. Oscillator 30 provides a reference signal labelled "F_{REF}" at a reference frequency to counter 14. Counter 14 provides a first signal labelled "F1" to phase detector 18, and receives sixteen signals labelled "LATCHR0-LATCHR15" and a signal labelled "JAM LOAD" from storage and control portion 12. Microprocessor 32 provides three signals, "DATA", "CLOCK", and "$\overline{\text{ENABLE}}$" to storage and control portion 12. Counter 16 receives sixteen latch signals "LATCHN0-LATCHN15" and JAM LOAD from storage and control portion 12. Counter 16 also receives an output signal labelled "FR_{OUT}" from voltage controlled oscillator 22, and provides a second signal labelled "F2" to phase detector 18. Phase detector 18 receives F1 and F2 and provides an phase detect output signal labelled "PD_{OUT}" to filter 20. Filter 20 receives PD_{OUT} and generates a filtered signal labelled "$FILTER_{OUT}$". Voltage controlled oscillator 22 receives $FILTER_{OUT}$ and provides FR_{OUT} in response.

In operation, phase locked loop 10 generates FR_{OUT} at a programmable frequency in response to a frequency of reference signal F_{REF} and two 16-bit numbers. Microprocessor 32 receives one or more instructions to send a first number or a second number through a serial microprocessor port. Microprocessor 32 provides input signals DATA, CLOCK, and $\overline{\text{ENABLE}}$ in response to the instruction or instructions. $\overline{\text{ENABLE}}$ is asserted, and 17 bits are provided serially on DATA by microprocessor 32, one bit per each CLOCK cycle. The first bit is an address bit to determine whether the first number or the second number follows. The following sixteen bits is the input number.

After receiving the address bit, storage and control portion 12 shifts each bit on DATA into a shift register. When the sixteenth bit of the input number is received, storage and control portion 12 stores the input number in a corresponding latch (not shown in FIG. 1). A latch associated with the first number provides signals LATCHR0–LATCHR15, and a latch associated with the second number provides signals LATCHN0-LATCHN15. Since CLOCK and F_{REF} are asynchronous with respect to each other, an incorrect value may be read if either counter tries to read the value of the latch while the number is being stored in the latch. However, JAM LOAD is asserted following reception of an input number, and causes counter 14 and counter 16 to reload the first number and the second number, respectively, solving the first problem.

Counter 14 is loaded with the first number and decrements once for each cycle of F_{REF}. Counter 14 provides F1 at a logic low until counter 14 reaches terminal count, provides F1 at a logic high, then automatically reloads the first predetermined number on LATCHR0-LATCHR15 and provides F1 again as a logic low. Similarly, counter 16 is loaded with the second number and decrements once for each cycle of FR_{OUT}. Counter 16 provides F2 at a logic low until counter 16 reaches terminal count, provides F2 at a logic high, and then automatically reloads the second predetermined number on LATCHN0-LATCHN16 and provides F2 as at a logic low. Both cycles repeat indefinitely.

Phase detector 18 receives F1 and F2 and generates PD_{OUT} as a phase difference between F1 and F2. If F1 and F2 are both a logic low, then PD_{OUT} is provided at a high impedance state. If F1 is high when F2 is low, PD_{OUT} is provided at a logic high; if F1 is low when F2 is high, PD_{OUT} is provided at a logic low. If both F1 and F2 are at a logic high, a state machine in phase detector 18 is reset asynchronously to the "00" state corresponding to F1 and F2 each being at a logic low. Filter 20 is a low pass filter, and provides an output signal $FILTER_{OUT}$ whose magnitude is proportional to the average value of PD_{OUT}. If PD_{OUT} is provided as a logic high, then the magnitude of $FILTER_{OUT}$ increases; if PD_{OUT} is provided as a logic low, the magnitude of $FILTER_{OUT}$ decreases; and if PD_{OUT} provided in a high impedance state, the magnitude of $FILTER_{OUT}$ stays substantially constant. $FILTER_{OUT}$ is then received by voltage controlled oscillator 22 and FR_{OUT} is generated at a frequency proportional to the voltage level of $FILTER_{OUT}$. The frequency of FR_{OUT} stabilizes when F1 and F2 are substantially the same.

Together, counter 16, phase detector 18, filter 20, and voltage controlled oscillator 22 provide a phase locked loop which, when used in conjunction with counter 14 receiving F_{REF}, allows the user to provide a digitally controlled output signal at a programmable frequency. The programmable frequency is determined by the values of F_{REF}, the first number, and the second number.

When storage and control portion 12 receives a new value for either the first number or the second number, counters 14 and 16 provide both F1 and F2 as a logic high. In response to F1 and F2 being provided in a logic high state, counter 14 and counter 16 load the counter values from LATCHR0-15 and LATCHN0-15, respectively. Providing F1 and F2 in this manner solves four problems associated with using a digital phase detector in PLL frequency synthesizers and like circuits having programmable divide ratios. The four problems are detailed below.

First, counters 14 and 16 periodically reload the first and second numbers from storage and control portion 12 every time the counters decrement to zero (known as terminal count). However CLOCK, used by microprocessor 32 to load the first and second numbers, is asynchronous to both F_{REF} and FR_{OUT}. Occasionally, therefore, an input number is being latched when a counter tries to read it, resulting in an incorrect, indeterminate value being read by the counter. The correct value is loaded the next time the counter reads the number, but until then, FR_{OUT} is incorrect and cannot begin to lock. One solution would be to load the data when the counters are not loading, but this solution increases the cost of the PLL by increasing the number of pins because a "COUNTER LOADING" signal must be provided. In addition, the MPU must monitor the COUNTER LOADING signal which increases software complexity.

Second, when an input number is provided by microprocessor 32, and the first problem does not occur, a large amount of time may be required before a corresponding counter reloads the number. If microprocessor 32 updates the counter value shortly after the counter reloads the number from storage and control portion 12, then the amount of time using an old counter value is relatively large. This problem is worse when the frequency of FR_{OUT} is to be changed from low to high, because the counter value for the low frequency is much greater. Having to wait up to a full counter cycle degrades performance and increases lock time.

Third, phase detector 18 is implemented as a state machine with two state variables. When the state machine is in state "00", then neither counter 14 nor counter 16 has reached terminal count. When a counter reaches terminal count, counter 14 or counter 16 asserts a F1 or F2, respectively, to phase detector 18. If the terminal count signal of one counter is asserted before the terminal count signal of the other counter, then the state machine goes into a "10" or "01" state. Filter 20 and voltage controlled oscillator 22 use this state informatin to adjust the output frequency until the other counter reaches terminal count. When both F1 and F2 have been asserted, then the state machine enters the "11" state which resets the state machine to the "00" state, and keeps the frequency of FR_{OUT} constant. Each counter loads a value when terminal count is reached, or on the assertion of F1 or F2, respectively. A problem occurs when a new value for either the first number or the second number is loaded when the phase detector is in a state other than "00". In this case, lock times increase when a new value is loaded.

Fourth, when an input number is received, the counter 14 and counter 16 are not likely to be synchronized, i.e., both asserting terminal count, when the value changes. In order to minimize lock times, both counter 14 and counter 16 should begin decrementing at the same time. Phase locked loop 10 solves each of these four problems, in a manner made clear by considering FIG. 2 and FIG. 3.

FIG. 2 shows a schematic of a phase detector 40 used in the phase locked loop of FIG. 1. Phase detector 40 comprises a flip-flop 42, a flip-flop 44, an inverter 46, an inverter 48, an inverter 50, an inverter 52, an inverter 54, a NAND gate 56, an inverter 57, a P-channel transistor 58, and an N-channel transistor 60. Flip-flop 42 has a clock input terminal labelled "CLK" receiving F1, a D input coupled to a first power supply voltage terminal labelled "V_{DD}", a reset terminal, and an inverted output terminal labelled "$\overline{Q}$" . V_{DD} is a positive power supply voltage terminal and is approximately 5 volts. Flip-flop 44 has a clock input terminal labelled "CLK" receiving F2, a D input coupled to VDD, a reset terminal, and an inverted output terminal labelled "$\overline{Q}$". Inverter 46 has an input terminal coupled to the inverted output terminal of first flip-flop 42, and an output terminal. Inverter 48 has an input terminal coupled to the output terminal of inverter 46, and an output terminal for providing a first phase output signal labelled "PHIR". Inverter 50 has an input terminal coupled to the inverted output terminal of second flip-flop 44, and an output terminal. Inverter 52 has an input terminal coupled to the output terminal of inverter 50, and an output terminal for providing a second phase output

signal labelled "PHIV". Inverter 54 has an input terminal coupled to the output terminal of inverter 52, and an output terminal. NAND gate 56 has a first input terminal coupled to the output terminal of inverter 46, a second input terminal coupled to the output terminal of inverter 50, and an output terminal. Inverter 57 has an input terminal coupled to the output terminal of NAND gate 56, and an output terminal coupled to the reset terminal of flip-flop 42 and to the reset terminal of flip-flop 44. Transistor 58 a first current electrode coupled to VDD, a control electrode coupled to the output terminal of inverter 48, and a second current electrode for providing a phase detect output signal labelled "PDOUT". Transistor 60 has a first current electrode coupled to the second current electrode of transistor 58, a control electrode coupled to the output terminal of inverter 54, and a second current electrode coupled to a second power supply voltage terminal labelled "V_{SS}". V_{SS}, is a negative power supply voltage terminal and is approximately 0 volts.

In operation, the output terminals of inverters 46 and 50 provide signals equivalant to the Q outputs of flip-flops 42 and 44, respectively. NAND gate 56 with inverter 57 provides an AND function. Therefore, flip-flops 42 and 44 are reset when F1 and F2 are both asserted (at a logic high), and the inverted outputs return to a logic high. Flip-flops 42 and 44 are edge-triggered, so that once set, the flip-flops remain set until they are reset. When F1 is asserted when F2 is negated, phase detector 40 provides PD_{OUT} at a logic high level. This logic high level increases the voltage on $FILTER_{OUT}$, increasing the frequency of FR_{OUT}. PD_{OUT} remains at a logic high level until F2 is asserted. When F1 is negated when F2 is asserted, phase detector provides PD_{OUT} at a logic low level. This logic low level decreases the voltage on $FILTER_{OUT}$, decreasing the frequency of FR_{OUT}. PD_{OUT} remains at a logic low level until F1 is asserted. When F1 and F2 are both negated, and flip-flops 42 and 44 are in the reset state, PD_{OUT} is in a high impedance state, which keeps the voltage on $FILTER_{OUT}$ and the frequency of FR_{OUT} substantially constant.

An important measure of performance of a phase locked loop is the lock time, that is, how long from a change of the first or second numbers until the frequency of FR_{OUT} substantially equals the desired frequency. Furthermore, in a digital phase detector, the lock time of the loop depends on the initial conditions of the phase detector. When the frequency is changed, F1 and F2 are forced into a logic high state by the assertion of JAM LOAD by storage and control portion 12, which puts the flip-flops back into the "00" state (solving the third problem). Since the counters reload the input numbers when F1 and F2 are both at a logic high, they are now synchronized upon a change in the input number (the fourth problem). Also the counters automatically reload their corresponding numbers whenever a number is changed (the second problem).

FIG. 3 shows a timing diagram of various signals of phase locked loop 10 useful in understanding the operation. All reference numbers pertain to FIG. 1. Microprocessor 32 asserts $\overline{\text{ENABLE}}$ to program phase locked loop 10. A CLOCK signal is also provided, which is a digital clock signal with approximately 50% duty cycle. Not shown in FIG. 3 is the stream of bits on DATA, which includes an address bit followed by sixteen data bits of the input number. On the falling edge of the CLOCK cycle corresponding to the sixteenth bit of the input number, storage and control portion 12 may assert a signal labelled "INHIBIT REPETITIVE LOAD" to counters 14 and 16, to prevent a load from occuring when the value of either the first latch or the second latch is changing. A signal labelled "LOAD N LATCH" is provided internally by storage and control portion 12 to cause the second latch to receive the input number from the shift register. Finally, JAM LOAD is asserted to ensure that counters 14 and 16 load new values. In the preferred embodiment, INHIBIT REPETITIVE LOAD is not necessary; in certain integrated circuit technologies, like fast CMOS processes, signal JAM LOAD is valid very soon after the rising edge of $\overline{\text{ENABLE}}$.

The manner of generating F1 and F2 eliminates the contention problem with the counters (the first problem). Storage and control portion 12 provides a signal labelled "INHIBIT REPETITIVE LOAD" to counters 14 and 16 so that when storage and control portion 12 is providing a new number to the first latch or the second latch, counter 14 and counter 16 do not assert F1 and F2. A ripple counter counts to 16 and then asserts INHIBIT REPETITIVE LOAD for one cycle, during which time the input number is stabilizing in the latch. Subsequently, after the last cycle in which the microprocessor is writing the input number to storage and control portion 12, a signal labelled JAM LOAD is asserted to force counters 14 and 16 to assert F1 and F2, respectively. Together, signals INHIBIT REPETITIVE LOAD and JAM LOAD ensure that contention is avoided.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

I claim:

1. A phase locked loop comprising:

input means, for storing first and second predetermined numbers in response to a plurality of input signals;

first counter means coupled to said input means, for receiving a reference signal, for storing said first predetermined number, for providing a first signal in response to either an occurrence of substantially said first predetermined number of cycles of said reference signal or to said input means storing either said first or said second predetermined number;

second counter means coupled to said input means, for receiving an output signal, for storing said second predetermined number, for providing a second signal in response to either an occurrence of substantially said second predetermined number of cycles of said output signal or to said input means storing either said first or said second predetermined number;

a phase detector coupled to said first counter means and to said second counter means, for providing a phase detect output signal in response to a difference in logic state between said first and second signals;

filter means coupled to said phase detector, for providing a filtered signal having a voltage proportional to a length of time said phase detector output signal is in a predetermined logic state; and

a voltage controlled oscillator, coupled to said filter means and said second counter, for providing said output signal having a frequency proportional to said voltage of said filtered signal.

2. The phase locked loop of claim 1 wherein said first counter means updates said first predetermined number in response to said first signal, and wherein said second counter means updates said second predetermined number in response to said second signal.

3. The phase locked loop of claim 2 wherein said phase detector comprises:

a first flip-flop, having a clock input receiving said first load signal, a D input coupled to a signal in a logic high state, a reset terminal, and an inverted output terminal;

a second flip-flop, having a clock input receiving said second load signal, a D input coupled to a signal in a logic high state, a reset terminal, and an inverted output terminal;

a first inverter, having an input terminal coupled to said inverted output terminal of said first flip-flop, and an output terminal;

a second inverter, having an input terminal coupled to said output terminal of said first inverter, and an output terminal for providing a first phase output signal;

a third inverter, having an input terminal coupled to said inverted output terminal of said second flip-flop, and an output terminal;

a fourth inverter, having an input terminal coupled to said output terminal of said third inverter, and an output terminal for providing a second phase output signal;

a fifth inverter, having an input terminal coupled to said output terminal of said fourth inverter, and an output terminal;

an AND gate, having a first input terminal coupled to said output terminal of said first inverter, a second input terminal coupled to said output terminal of said third inverter, and an output terminal coupled to said reset terminal of said first flip-flop and to said reset terminal of said second flip-flop;

a first transistor, having a first current electrode coupled to a first power supply voltage terminal, a control electrode coupled to said output terminal of said second inverter, and a second current electrode for providing said phase detect output signal; and

a second transistor, having a first current electrode coupled to the second current electrode of said first transistor, a control electrode coupled to said output terminal of said fifth inverter, and a second current electrode coupled to a second power supply voltage terminal.

4. The phase locked loop of claim 3, wherein said first power supply voltage terminal is a positive power supply voltage terminal, and wherein said second power supply voltage terminal is a negative power supply voltage terminal.

5. The phase locked loop of claim 1, wherein said predetermined logic state is a logic high.

6. A phase locked loop comprising:

input means, for storing first and second predetermined numbers in response to a plurality of input signals;

reference means coupled to said input means, for providing a first signal in response to counting substantially said first predetermined number of cycles of a reference signal, for providing a second signal in response to counting substantially said second predetermined number of cycles of an output signal, and for providing both said first signal and said second signal in response to said input means storing either said first predetermined number or said second predetermined number;

phase detection means coupled to said reference means, for providing a phase difference signal in response to a difference in logic state between said first signal and said second signal; and

loop means coupled to said phase detection means and to said reference means, for providing said output signal having a frequency proportional to said phase difference signal.

7. The phase locked loop of claim 6, wherein said reference means updates said first predetermined number in response to providing said first signal, and updates said second predetermined number in response to providing said second signal.

8. The phase locked loop of claim 6, wherein said first signal and said second signal are digital signals.

9. The phase locked loop of claim 8, wherein said predetermined logic state is a logic high.

10. A method of providing an output signal having a programmable frequency comprising the steps of:

providing a first signal in response to an occurrence of a first predetermined number of cycles of a reference signal;

providing a second signal in response to an occurrence of a second predetermined number of cycles of the output signal;

providing both said first signal and said second signal in response to a change in either said first predetermined number or said second predetermined number;

providing a phase detect signal having a duty cycle proportional to a detected phase difference between said first signal and said second signal;

providing a filtered signal having a voltage proportional to said duty cycle; and

providing the output signal having a frequency proportional to said voltage of said phase detect signal.

* * * * *

Exhibit A

United States Patent [19]

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[11] **Patent Number: 4,951,005**

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[54] **PHASE LOCKED LOOP WITH REDUCED FREQUENCY/PHASE LOCK TIME**

[75] Inventor: **David C. Babin**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

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[58] **Field of Search** ..... 331/1 A, 16, 18, 25, 331/27; 455/260

[56] **References Cited**

U.S. PATENT DOCUMENTS

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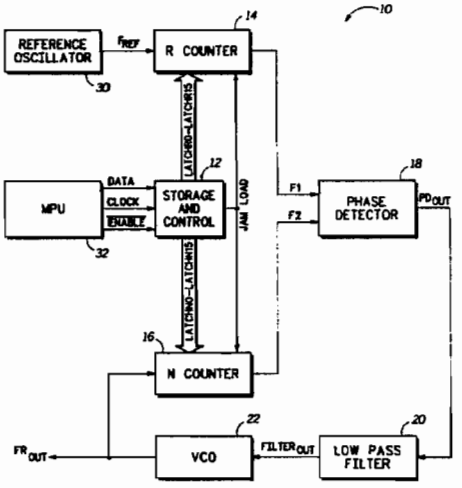
Primary Examiner—David Mis

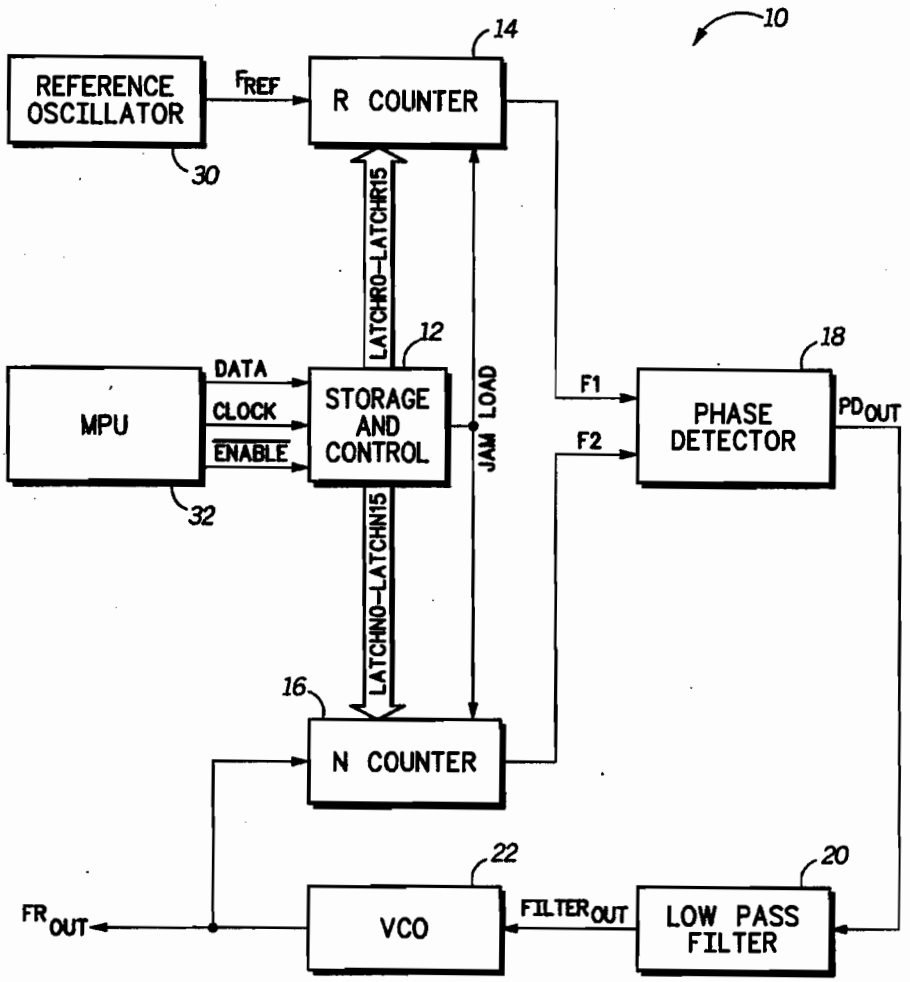
Attorney, Agent, or Firm—Robert L. King; Paul J. Polansky

[57] **ABSTRACT**

A phase locked loop for providing a programmable frequency output signal with reduced phase-frequency lock time. A phase detector detects a phase difference between a reference frequency divided by a first number, and a frequency of the output signal divided by a second number. First and second counters receive the first and the second input numbers to divide a respective frequency. Whenever an input number is loaded, a load signal resets the phase detector and causes each counter to be loaded, which reduces the lock time of the loop.

10 Claims, 2 Drawing Sheets

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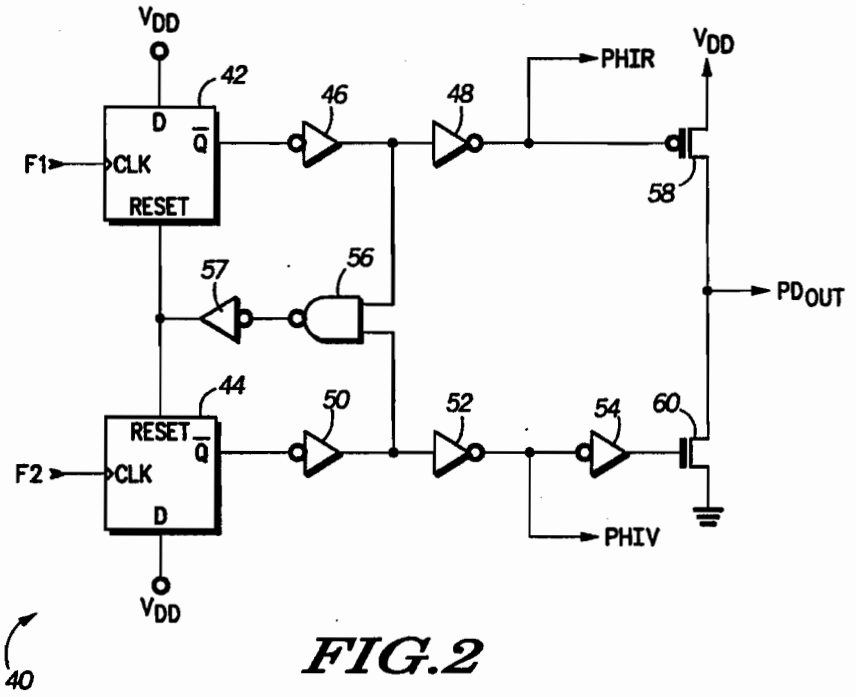
14
REFERENCE OSCILLATOR
FREF
R COUNTER
30
LATCHR0–LATCHR15
12
18
DATA
CLOCK
ENABLE
MPU
STORAGE AND CONTROL
JAM LOAD
F1
F2
PHASE DETECTOR
PDOUT
32
LATCHN0–LATCHN15
16
N COUNTER
22
20
FROUT
VCO
FILTEROUT
LOW PASS FILTER

FIG. 1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D
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F1
CLK
RESET
46
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PHIR
VDD
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PDOUT
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RESET
Q
F2
CLK
D
50
52
54
60
PHIV
VDD
40

FIG.2

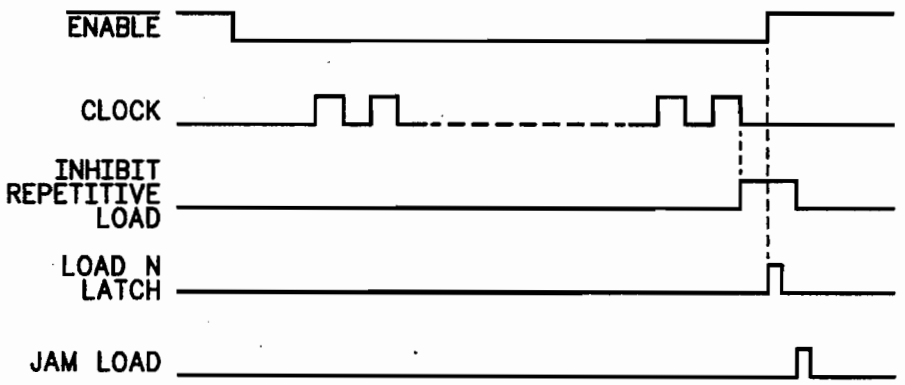
ENABLE
CLOCK
INHIBIT REPETITIVE LOAD
LOAD N LATCH
JAM LOAD

FIG.3

PHASE LOCKED LOOP WITH REDUCED FREQUENCY/PHASE LOCK TIME

FIELD OF THE INVENTION

This invention relates generally to phase locked loops, and more particularly, to programmable, digital phase locked loops used for frequency synthesizers.

BACKGROUND OF THE INVENTION

Phase locked loops (PLLs) have important uses in communications applications. A PLL frequency synthesizer, one such use, generates an output signal having a programmable frequency to be used in tuning of two or more communication channels. Typically, a microprocessor programs the frequency of the output signal. In many applications, the programmed frequency must change dynamically. For example, the frequency normally generated by the PLL frequency synthesizer is used to tune a communications signal, but periodically the frequency must be changed to tune an auxiliary channel. The functioning of the phase locked loop may be enhanced by using a digital phase detector to measure a phase difference between the output signal and a proportion of a reference signal, and to adjust the output signal in response to a detected phase difference. Performance of PLL frequency synthesizers using digital phase detectors must continually be improved to meet increased performance requirements of communication circuits.

BRIEF DESCRIPTION OF THE INVENTION

Accordingly, it is an object of the present invention to provide a phase locked loop with improved lock time.

It is another object of the present invention to provide a phase locked loop with an improved phase detection mechanism.

In carrying out these and other objects of the invention, there is provided, in one form, a phase locked loop comprising an input portion, a reference portion, a phase detection portion, and a loop portion. The input portion stores a first and a second predetermined number in response to a plurality of input signals. The reference portion is coupled to the input portion, and provides a first signal in response to the first predetermined number of cycles of a reference signal, a second signal in response to the second predetermined number of cycles of an output signal, and both the first signal and the second signal in response to the input portion storing either the first predetermined number or the second predetermined number. The phase detection portion is coupled to the reference portion, and provides a phase difference signal in response to a difference in logic state between the first signal and the second signal. The loop portion is coupled to the phase detection portion and to the reference portion, and provides the output signal as a frequency proportional to the phase difference signal.

These and other objects, features and advantages will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates in block diagram form a phase locked loop in accordance with a preferred embodiment of the present invention;

FIG. 2 shows a schematic of a phase detector used in the phase locked loop of FIG. 1; and

FIG. 3 shows a timing diagram useful in understanding the phase locked loop of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates in block diagram form a phase locked loop 10 in accordance with a preferred embodiment of the present invention. Phase locked loop 10 comprises a storage and control portion 12, an R counter 14, an N counter 16, a phase detector 18, a low pass filter 20, and a voltage controlled oscillator (VCO) 22. Also shown are a reference oscillator 30, and a microprocessor (MPU) 32, which are not a part of phase locked loop 10. Oscillator 30 provides a reference signal labelled "F_{REF}" at a reference frequency to counter 14. Counter 14 provides a first signal labelled "F1" to phase detector 18, and receives sixteen signals labelled "LATCHR0-LATCHR15" and a signal labelled "JAM LOAD" from storage and control portion 12. Microprocessor 32 provides three signals, "DATA", "CLOCK", and "$\overline{\text{ENABLE}}$" to storage and control portion 12. Counter 16 receives sixteen latch signals "LATCHN0-LATCHN15" and JAM LOAD from storage and control portion 12. Counter 16 also receives an output signal labelled "FR_{OUT}" from voltage controlled oscillator 22, and provides a second signal labelled "F2" to phase detector 18. Phase detector 18 receives F1 and F2 and provides an phase detect output signal labelled "PD_{OUT}" to filter 20. Filter 20 receives PD_{OUT} and generates a filtered signal labelled "$FILTER_{OUT}$". Voltage controlled oscillator 22 receives $FILTER_{OUT}$ and provides FR_{OUT} in response.

In operation, phase locked loop 10 generates FR_{OUT} at a programmable frequency in response to a frequency of reference signal F_{REF} and two 16-bit numbers. Microprocessor 32 receives one or more instructions to send a first number or a second number through a serial microprocessor port. Microprocessor 32 provides input signals DATA, CLOCK, and $\overline{\text{ENABLE}}$ in response to the instruction or instructions. $\overline{\text{ENABLE}}$ is asserted, and 17 bits are provided serially on DATA by microprocessor 32, one bit per each CLOCK cycle. The first bit is an address bit to determine whether the first number or the second number follows. The following sixteen bits is the input number.

After receiving the address bit, storage and control portion 12 shifts each bit on DATA into a shift register. When the sixteenth bit of the input number is received, storage and control portion 12 stores the input number in a corresponding latch (not shown in FIG. 1). A latch associated with the first number provides signals LATCHR0–LATCHR15, and a latch associated with the second number provides signals LATCHN0-LATCHN15. Since CLOCK and F_{REF} are asynchronous with respect to each other, an incorrect value may be read if either counter tries to read the value of the latch while the number is being stored in the latch. However, JAM LOAD is asserted following reception of an input number, and causes counter 14 and counter 16 to reload the first number and the second number, respectively, solving the first problem.

Counter 14 is loaded with the first number and decrements once for each cycle of F_{REF}. Counter 14 provides F1 at a logic low until counter 14 reaches terminal count, provides F1 at a logic high, then automatically reloads the first predetermined number on LATCHR0-LATCHR15 and provides F1 again as a logic low. Similarly, counter 16 is loaded with the second number and decrements once for each cycle of FR_{OUT}. Counter 16 provides F2 at a logic low until counter 16 reaches terminal count, provides F2 at a logic high, and then automatically reloads the second predetermined number on LATCHN0-LATCHN16 and provides F2 as at a logic low. Both cycles repeat indefinitely.

Phase detector 18 receives F1 and F2 and generates PD_{OUT} as a phase difference between F1 and F2. If F1 and F2 are both a logic low, then PD_{OUT} is provided at a high impedance state. If F1 is high when F2 is low, PD_{OUT} is provided at a logic high; if F1 is low when F2 is high, PD_{OUT} is provided at a logic low. If both F1 and F2 are at a logic high, a state machine in phase detector 18 is reset asynchronously to the "00" state corresponding to F1 and F2 each being at a logic low. Filter 20 is a low pass filter, and provides an output signal $FILTER_{OUT}$ whose magnitude is proportional to the average value of PD_{OUT}. If PD_{OUT} is provided as a logic high, then the magnitude of $FILTER_{OUT}$ increases; if PD_{OUT} is provided as a logic low, the magnitude of $FILTER_{OUT}$ decreases; and if PD_{OUT} provided in a high impedance state, the magnitude of $FILTER_{OUT}$ stays substantially constant. $FILTER_{OUT}$ is then received by voltage controlled oscillator 22 and FR_{OUT} is generated at a frequency proportional to the voltage level of $FILTER_{OUT}$. The frequency of FR_{OUT} stabilizes when F1 and F2 are substantially the same.

Together, counter 16, phase detector 18, filter 20, and voltage controlled oscillator 22 provide a phase locked loop which, when used in conjunction with counter 14 receiving F_{REF}, allows the user to provide a digitally controlled output signal at a programmable frequency. The programmable frequency is determined by the values of F_{REF}, the first number, and the second number.

When storage and control portion 12 receives a new value for either the first number or the second number, counters 14 and 16 provide both F1 and F2 as a logic high. In response to F1 and F2 being provided in a logic high state, counter 14 and counter 16 load the counter values from LATCHR0-15 and LATCHN0-15, respectively. Providing F1 and F2 in this manner solves four problems associated with using a digital phase detector in PLL frequency synthesizers and like circuits having programmable divide ratios. The four problems are detailed below.

First, counters 14 and 16 periodically reload the first and second numbers from storage and control portion 12 every time the counters decrement to zero (known as terminal count). However CLOCK, used by microprocessor 32 to load the first and second numbers, is asynchronous to both F_{REF} and FR_{OUT}. Occasionally, therefore, an input number is being latched when a counter tries to read it, resulting in an incorrect, indeterminate value being read by the counter. The correct value is loaded the next time the counter reads the number, but until then, FR_{OUT} is incorrect and cannot begin to lock. One solution would be to load the data when the counters are not loading, but this solution increases the cost of the PLL by increasing the number of pins because a "COUNTER LOADING" signal must be provided. In addition, the MPU must monitor the COUNTER LOADING signal which increases software complexity.

Second, when an input number is provided by microprocessor 32, and the first problem does not occur, a large amount of time may be required before a corresponding counter reloads the number. If microprocessor 32 updates the counter value shortly after the counter reloads the number from storage and control portion 12, then the amount of time using an old counter value is relatively large. This problem is worse when the frequency of FR_{OUT} is to be changed from low to high, because the counter value for the low frequency is much greater. Having to wait up to a full counter cycle degrades performance and increases lock time.

Third, phase detector 18 is implemented as a state machine with two state variables. When the state machine is in state "00", then neither counter 14 nor counter 16 has reached terminal count. When a counter reaches terminal count, counter 14 or counter 16 asserts a F1 or F2, respectively, to phase detector 18. If the terminal count signal of one counter is asserted before the terminal count signal of the other counter, then the state machine goes into a "10" or "01" state. Filter 20 and voltage controlled oscillator 22 use this state informatin to adjust the output frequency until the other counter reaches terminal count. When both F1 and F2 have been asserted, then the state machine enters the "11" state which resets the state machine to the "00" state, and keeps the frequency of FR_{OUT} constant. Each counter loads a value when terminal count is reached, or on the assertion of F1 or F2, respectively. A problem occurs when a new value for either the first number or the second number is loaded when the phase detector is in a state other than "00". In this case, lock times increase when a new value is loaded.

Fourth, when an input number is received, the counter 14 and counter 16 are not likely to be synchronized, i.e., both asserting terminal count, when the value changes. In order to minimize lock times, both counter 14 and counter 16 should begin decrementing at the same time. Phase locked loop 10 solves each of these four problems, in a manner made clear by considering FIG. 2 and FIG. 3.

FIG. 2 shows a schematic of a phase detector 40 used in the phase locked loop of FIG. 1. Phase detector 40 comprises a flip-flop 42, a flip-flop 44, an inverter 46, an inverter 48, an inverter 50, an inverter 52, an inverter 54, a NAND gate 56, an inverter 57, a P-channel transistor 58, and an N-channel transistor 60. Flip-flop 42 has a clock input terminal labelled "CLK" receiving F1, a D input coupled to a first power supply voltage terminal labelled "V_{DD}", a reset terminal, and an inverted output terminal labelled "$\overline{Q}$" . V_{DD} is a positive power supply voltage terminal and is approximately 5 volts. Flip-flop 44 has a clock input terminal labelled "CLK" receiving F2, a D input coupled to VDD, a reset terminal, and an inverted output terminal labelled "$\overline{Q}$". Inverter 46 has an input terminal coupled to the inverted output terminal of first flip-flop 42, and an output terminal. Inverter 48 has an input terminal coupled to the output terminal of inverter 46, and an output terminal for providing a first phase output signal labelled "PHIR". Inverter 50 has an input terminal coupled to the inverted output terminal of second flip-flop 44, and an output terminal. Inverter 52 has an input terminal coupled to the output terminal of inverter 50, and an output terminal for providing a second phase output

signal labelled "PHIV". Inverter 54 has an input terminal coupled to the output terminal of inverter 52, and an output terminal. NAND gate 56 has a first input terminal coupled to the output terminal of inverter 46, a second input terminal coupled to the output terminal of inverter 50, and an output terminal. Inverter 57 has an input terminal coupled to the output terminal of NAND gate 56, and an output terminal coupled to the reset terminal of flip-flop 42 and to the reset terminal of flip-flop 44. Transistor 58 a first current electrode coupled to VDD, a control electrode coupled to the output terminal of inverter 48, and a second current electrode for providing a phase detect output signal labelled "PDOUT". Transistor 60 has a first current electrode coupled to the second current electrode of transistor 58, a control electrode coupled to the output terminal of inverter 54, and a second current electrode coupled to a second power supply voltage terminal labelled "V_{SS}". V_{SS}, is a negative power supply voltage terminal and is approximately 0 volts.

In operation, the output terminals of inverters 46 and 50 provide signals equivalant to the Q outputs of flip-flops 42 and 44, respectively. NAND gate 56 with inverter 57 provides an AND function. Therefore, flip-flops 42 and 44 are reset when F1 and F2 are both asserted (at a logic high), and the inverted outputs return to a logic high. Flip-flops 42 and 44 are edge-triggered, so that once set, the flip-flops remain set until they are reset. When F1 is asserted when F2 is negated, phase detector 40 provides PD_{OUT} at a logic high level. This logic high level increases the voltage on $FILTER_{OUT}$, increasing the frequency of FR_{OUT}. PD_{OUT} remains at a logic high level until F2 is asserted. When F1 is negated when F2 is asserted, phase detector provides PD_{OUT} at a logic low level. This logic low level decreases the voltage on $FILTER_{OUT}$, decreasing the frequency of FR_{OUT}. PD_{OUT} remains at a logic low level until F1 is asserted. When F1 and F2 are both negated, and flip-flops 42 and 44 are in the reset state, PD_{OUT} is in a high impedance state, which keeps the voltage on $FILTER_{OUT}$ and the frequency of FR_{OUT} substantially constant.

An important measure of performance of a phase locked loop is the lock time, that is, how long from a change of the first or second numbers until the frequency of FR_{OUT} substantially equals the desired frequency. Furthermore, in a digital phase detector, the lock time of the loop depends on the initial conditions of the phase detector. When the frequency is changed, F1 and F2 are forced into a logic high state by the assertion of JAM LOAD by storage and control portion 12, which puts the flip-flops back into the "00" state (solving the third problem). Since the counters reload the input numbers when F1 and F2 are both at a logic high, they are now synchronized upon a change in the input number (the fourth problem). Also the counters automatically reload their corresponding numbers whenever a number is changed (the second problem).

FIG. 3 shows a timing diagram of various signals of phase locked loop 10 useful in understanding the operation. All reference numbers pertain to FIG. 1. Microprocessor 32 asserts $\overline{\text{ENABLE}}$ to program phase locked loop 10. A CLOCK signal is also provided, which is a digital clock signal with approximately 50% duty cycle. Not shown in FIG. 3 is the stream of bits on DATA, which includes an address bit followed by sixteen data bits of the input number. On the falling edge of the CLOCK cycle corresponding to the sixteenth bit of the input number, storage and control portion 12 may assert a signal labelled "INHIBIT REPETITIVE LOAD" to counters 14 and 16, to prevent a load from occuring when the value of either the first latch or the second latch is changing. A signal labelled "LOAD N LATCH" is provided internally by storage and control portion 12 to cause the second latch to receive the input number from the shift register. Finally, JAM LOAD is asserted to ensure that counters 14 and 16 load new values. In the preferred embodiment, INHIBIT REPETITIVE LOAD is not necessary; in certain integrated circuit technologies, like fast CMOS processes, signal JAM LOAD is valid very soon after the rising edge of $\overline{\text{ENABLE}}$.

The manner of generating F1 and F2 eliminates the contention problem with the counters (the first problem). Storage and control portion 12 provides a signal labelled "INHIBIT REPETITIVE LOAD" to counters 14 and 16 so that when storage and control portion 12 is providing a new number to the first latch or the second latch, counter 14 and counter 16 do not assert F1 and F2. A ripple counter counts to 16 and then asserts INHIBIT REPETITIVE LOAD for one cycle, during which time the input number is stabilizing in the latch. Subsequently, after the last cycle in which the microprocessor is writing the input number to storage and control portion 12, a signal labelled JAM LOAD is asserted to force counters 14 and 16 to assert F1 and F2, respectively. Together, signals INHIBIT REPETITIVE LOAD and JAM LOAD ensure that contention is avoided.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

I claim:

1. A phase locked loop comprising:

input means, for storing first and second predetermined numbers in response to a plurality of input signals;

first counter means coupled to said input means, for receiving a reference signal, for storing said first predetermined number, for providing a first signal in response to either an occurrence of substantially said first predetermined number of cycles of said reference signal or to said input means storing either said first or said second predetermined number;

second counter means coupled to said input means, for receiving an output signal, for storing said second predetermined number, for providing a second signal in response to either an occurrence of substantially said second predetermined number of cycles of said output signal or to said input means storing either said first or said second predetermined number;

a phase detector coupled to said first counter means and to said second counter means, for providing a phase detect output signal in response to a difference in logic state between said first and second signals;

filter means coupled to said phase detector, for providing a filtered signal having a voltage proportional to a length of time said phase detector output signal is in a predetermined logic state; and

a voltage controlled oscillator, coupled to said filter means and said second counter, for providing said output signal having a frequency proportional to said voltage of said filtered signal.

2. The phase locked loop of claim 1 wherein said first counter means updates said first predetermined number in response to said first signal, and wherein said second counter means updates said second predetermined number in response to said second signal.

3. The phase locked loop of claim 2 wherein said phase detector comprises:

a first flip-flop, having a clock input receiving said first load signal, a D input coupled to a signal in a logic high state, a reset terminal, and an inverted output terminal;

a second flip-flop, having a clock input receiving said second load signal, a D input coupled to a signal in a logic high state, a reset terminal, and an inverted output terminal;

a first inverter, having an input terminal coupled to said inverted output terminal of said first flip-flop, and an output terminal;

a second inverter, having an input terminal coupled to said output terminal of said first inverter, and an output terminal for providing a first phase output signal;

a third inverter, having an input terminal coupled to said inverted output terminal of said second flip-flop, and an output terminal;

a fourth inverter, having an input terminal coupled to said output terminal of said third inverter, and an output terminal for providing a second phase output signal;

a fifth inverter, having an input terminal coupled to said output terminal of said fourth inverter, and an output terminal;

an AND gate, having a first input terminal coupled to said output terminal of said first inverter, a second input terminal coupled to said output terminal of said third inverter, and an output terminal coupled to said reset terminal of said first flip-flop and to said reset terminal of said second flip-flop;

a first transistor, having a first current electrode coupled to a first power supply voltage terminal, a control electrode coupled to said output terminal of said second inverter, and a second current electrode for providing said phase detect output signal; and

a second transistor, having a first current electrode coupled to the second current electrode of said first transistor, a control electrode coupled to said output terminal of said fifth inverter, and a second current electrode coupled to a second power supply voltage terminal.

4. The phase locked loop of claim 3, wherein said first power supply voltage terminal is a positive power supply voltage terminal, and wherein said second power supply voltage terminal is a negative power supply voltage terminal.

5. The phase locked loop of claim 1, wherein said predetermined logic state is a logic high.

6. A phase locked loop comprising:

input means, for storing first and second predetermined numbers in response to a plurality of input signals;

reference means coupled to said input means, for providing a first signal in response to counting substantially said first predetermined number of cycles of a reference signal, for providing a second signal in response to counting substantially said second predetermined number of cycles of an output signal, and for providing both said first signal and said second signal in response to said input means storing either said first predetermined number or said second predetermined number;

phase detection means coupled to said reference means, for providing a phase difference signal in response to a difference in logic state between said first signal and said second signal; and

loop means coupled to said phase detection means and to said reference means, for providing said output signal having a frequency proportional to said phase difference signal.

7. The phase locked loop of claim 6, wherein said reference means updates said first predetermined number in response to providing said first signal, and updates said second predetermined number in response to providing said second signal.

8. The phase locked loop of claim 6, wherein said first signal and said second signal are digital signals.

9. The phase locked loop of claim 8, wherein said predetermined logic state is a logic high.

10. A method of providing an output signal having a programmable frequency comprising the steps of:

providing a first signal in response to an occurrence of a first predetermined number of cycles of a reference signal;

providing a second signal in response to an occurrence of a second predetermined number of cycles of the output signal;

providing both said first signal and said second signal in response to a change in either said first predetermined number or said second predetermined number;

providing a phase detect signal having a duty cycle proportional to a detected phase difference between said first signal and said second signal;

providing a filtered signal having a voltage proportional to said duty cycle; and

providing the output signal having a frequency proportional to said voltage of said phase detect signal.

* * * * *

Exhibit B

United States Patent [19]

Littlebury

[11] **Patent Number: 5,008,615**

[45] **Date of Patent: Apr. 16, 1991**

[54] **MEANS AND METHOD FOR TESTING INTEGRATED CIRCUITS ATTACHED TO A LEADFRAME**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **431,346**

[22] Filed: **Nov. 3, 1989**

[51] Int. Cl.[5] G01R 1/06; G01R 31/02

[52] U.S. Cl. ..... 324/158 F; 324/158 P; 29/827

[58] Field of Search ..... 324/73.1, 158 R, 158 F; 357/70, 74; 174/52.4; 437/8; 29/827, 593; 361/401

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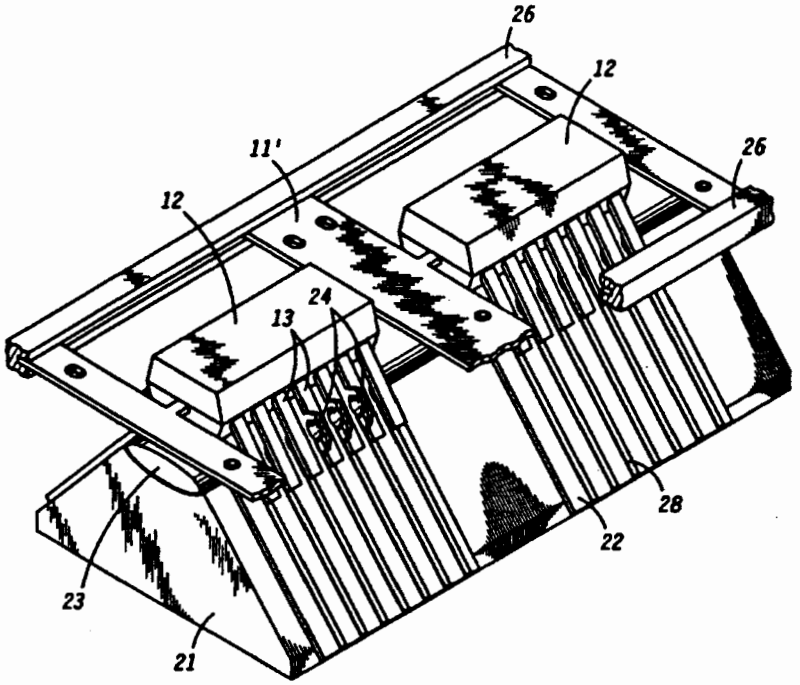
Primary Examiner—Kenneth Wieder
Assistant Examiner—Vinh P. Nguyen
Attorney, Agent, or Firm—Joe E. Barbee; Stuart T. Langley

[57] **ABSTRACT**

Apparatus and method of testing integrated circuits after the leads have been trimmed and partially formed, but before the package has been removed from the leadframe. One stage of a progressive trim and form process is adapted to test the integrated circuits by providing a membrane test head positioned underneath the IC package, wherein the membrane test head is coupled to an external tester. After the leads are electrically separated from each other end from the leadframe, the leads are aligned to the membrane test head and an inflatable bladder, which is positioned underneath the membrane test head, is inflated to couple the membrane test head to the leads. In this manner, one or more integrated circuits can be tested while still attached to the leadframe.

9 Claims, 2 Drawing Sheets



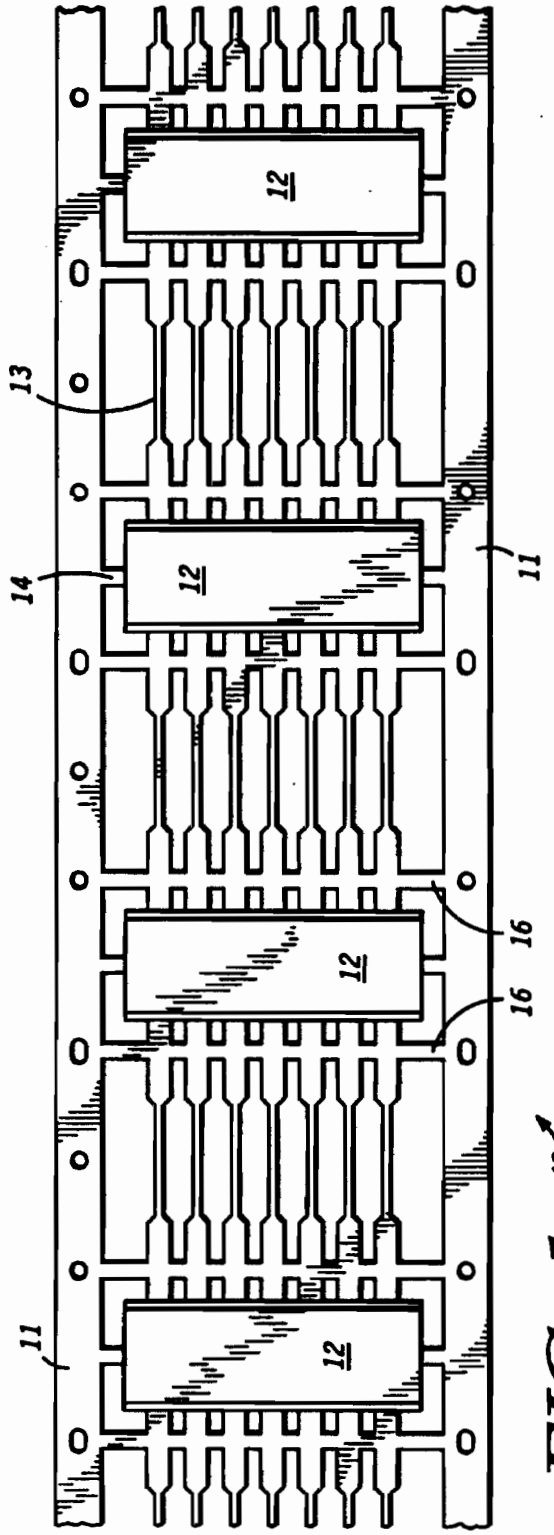


FIG. 1

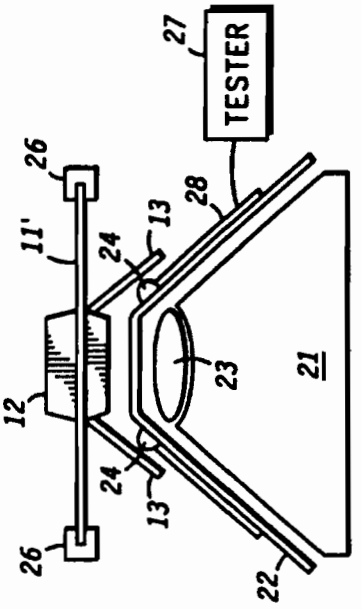


FIG. 3

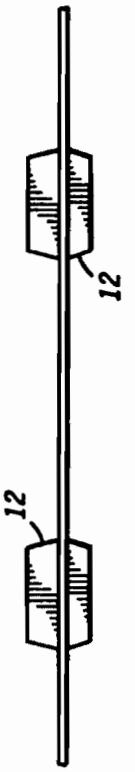


FIG. 2

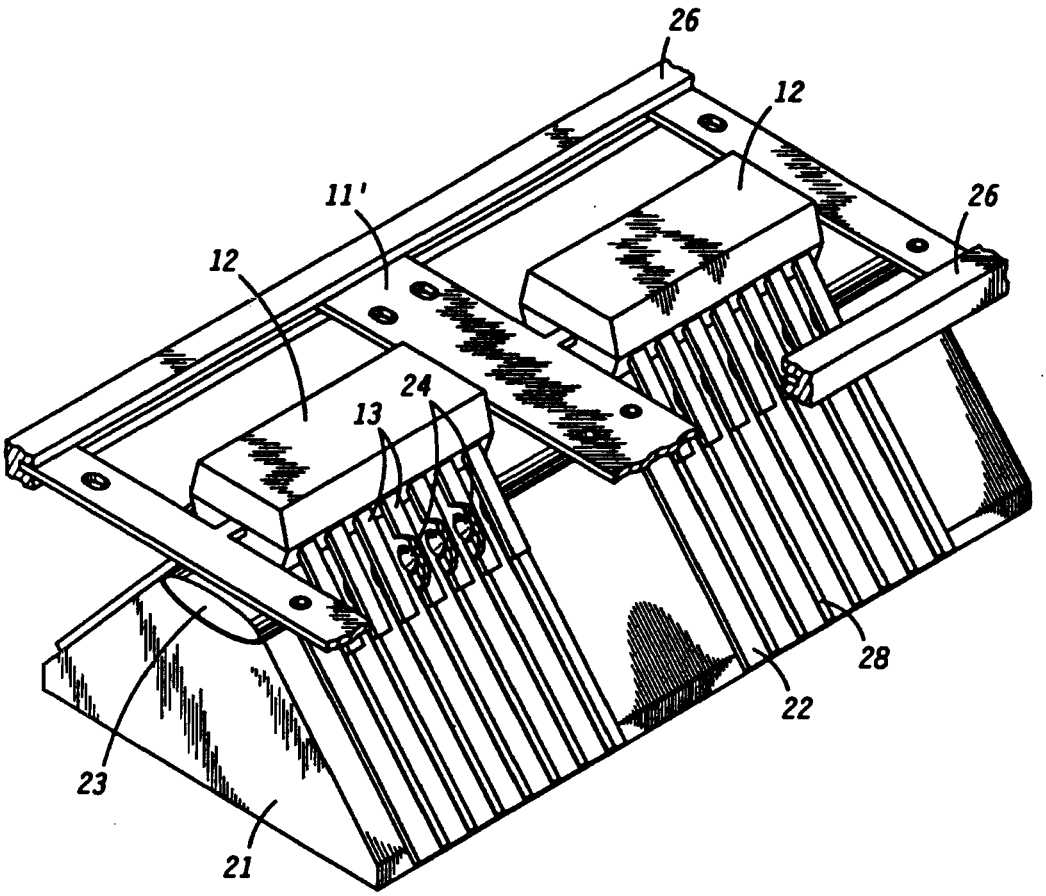


FIG. 4

MEANS AND METHOD FOR TESTING INTEGRATED CIRCUITS ATTACHED TO A LEADFRAME

BACKGROUND OF THE INVENTION

The present invention relates, in general, to methods of testing integrated circuits, and more particularly, to a method of testing integrated circuits which are attached to a leadframe.

To ensure functionality, integrated circuits (ICs) must be tested several times before they are shipped to a customer. Although most processes involved in manufacturing integrated circuits are batch processes in which many circuits are processed at a single time, testing has usually called for individual handling of the circuits. Integrated circuits are usually encapsulated on leadframes which comprise a plurality of circuits, but it has been necessary to separate the circuits from the leadframe to test them. Once the circuits are removed from the leadframe, they are particularly fragile, and leads which extend from the package are easily bent or torn. Stringent requirements for lead and package quality placed on manufacturers make it important to handle the packaged integrated circuits as little as possible once they are removed from the leadframe. These requirements are not congruent with the manufacturer's need to handle and test each of the integrated circuit packages individually.

IC packages are usually attached to a leadframe by the leads themselves and by tie-bars which couple package to the leadframe. The packages are trimmed from the leadframe in a trim and leadform tool which has several stages, each stage performing only part of the trim process. After the leads are trimmed so that they are mechanically separated from the leadframe and from each other, they are usually lead formed into a predetermined shape to meet a customer's specification. After the leadform is complete, the tie-bars are cut, separating the IC package from the leadframe completely. The trim and leadform operations are performed sequentially in the same tool so that damage to the leads and package resulting from handling is minimal.

At a stage in the trim/leadform process after the leads were electrically separated from the leadframe but before the packages were mechanically separated from the leadframe the ICs were electrically separate from each other so that testing could be done, yet it was impossible to make electrical contact to the package leads for testing. A major difficulty with testing devices which are still attached to a leadframe is making contact to a large number of half-formed pins or leads in the narrow confines of the trim and leadform tool. Conventional test head geometries cannot make contact in these conditions.

Although testing is designed to improve the reliability of integrated circuits, often it compromises the quality of packaged devices. Individual loading and unloading of integrated circuits into test fixtures often damaged leads which extend outside the integrated circuit package. This damage was usually not repairable and resulted in completely functional devices being rejected for physical quality problems. In addition to lead damage, package damage also occured. Also, handling of packaged integrated circuits increased the chances of damage to the circuits themselves by electrostatic discharge. Although testing is necessary to provide the desired reliability and functionality, the above mentioned quality limits have long been a costly problem for circuit manufacturers.

Accordingly, it is an object of the present invention to provide a means and method for testing integrated circuits which are attached to a leadframe.

It is another object of the present invention to provide a means and method for testing integrated circuits which reduces cycle time.

Another object of the present invention is to provide a means and method for testing integrated circuits which reduces testing cost.

A further object of the present invention is to provide a means and method for testing integrated circuits which eliminates individual handling of the integrated circuits.

Still another object of the present invention is to provide a method of testing integrated circuits which improves package quality.

SUMMARY OF THE INVENTION

These and other objects and advantages of the present invention are achieved by a method of testing integrated circuits after the leads have been trimmed and partially formed, but before the packages have been removed from the leadframe. One stage of a trim and form process is adapted to test the integrated circuits by providing a membrane test head positioned underneath the IC package, wherein the membrane test head is coupled to an external tester. After the leads are electrically separated from each other and from the leadframe, the leads are aligned to the membrane test head and an inflatable bladder which is positioned underneath the membrane test head, is inflated to couple the membrane test head to the leads. In this manner, one or more integrated circuits can be tested while still attached to the leadframe.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 illustrates a plan view of a portion of a leadframe on which integrated circuits are packaged;

FIG. 2 illustrates a side view of the leadframe shown in FIG. 1;

FIG. 3 illustrates a cross section of a tester of the present invention; and

FIG. 4 illustrates a cut away perspective view of the apparatus shown in FIG. 3.

DETAILED DESCRIPTION OF DRAWINGS

FIG. 1 shows a portion of a conventional leadframe used to package integrated circuits. Many packages 12 are formed on a leadframe, where each package 12 comprises an integrated circuit which is coupled to leads 13. FIG. 1 illustrates a leadframe after package 12 has been formed, encapsulating the integrated circuit chip. Package 12 provides mechanical support for leads 13 so they cannot be bent or deformed. Before encapsulation, however, tie-bar 16 must provide this mechanical support. Also, tie-bars 14 hold packages 12 to leadframe 11. Packages 12 may be oriented in a variety of ways on leadframe 11, for instance all packages 12 may be rotated 90° from the orientation shown in FIG. 1. Also, packages 12 may be interleaved to provide a tighter packing density. As will be seen, the testing method of the present invention can be modified to accommodate such variations.

FIG. 2 illustrates a side view of the leadframe shown in FIG. 1. As can be seen, packages 12 extend above and below leadframe 11 and leads 13, tie-bars 14 and 16, and side rails 11 all lie in the same plane. Spacing and orientation between packages 12 is fixed by the geometry of the leadframe.

In the past, the next step in processing of the leadframe shown in FIGS. 1 and 2 was to trim and leadform leads 13. This process was usually done in at least three stages. First, leads 13 were trimmed so that they were mechanically separate from each other and from leadframe 11. Next, leads 13 were leadformed into a predetermined shape which was specified by a customer. Lastly, tie-bars 14 were trimmed to separate packages 12 from leadframe 11. Conventionally, singulated packages 12 would then be transferred to a separate tester to evaluate functionality of the chip inside package 12.

FIG. 3 illustrates a cross-sectional view of a tester of the present invention. For ease of description, package 12 is shown with a different orientation with respect to leadframe 11' than shown in FIG. 1. The prime designation has been added in FIG. 3 to note this difference. Testing is performed in series with the trim and form process described hereinbefore. Testing is performed after mechanical separation of leads 13 yet before the leadform process is complete. Backing bar 21 provides a mechanical support for the rest of the test apparatus, and can be of any shape and material which adapts easily to the trim and leadform tool. A recess is formed in the top of backing bar 21 to hold inflatable bladder 23. Inflatable bladder 23 is a balloon-like bladder which can be inflated with gas or liquid. Membrane 22 is stretched over backing bar 21 and bladder 23. For ease of description, membrane 22 is shown separate from backing bar 21 and bladder 23, but it should be understood that in practice it is preferable that they rest against each other. Membrane 22 comprises a flexible printed circuit board such as UPILEX ®, which is a registered trademark of UBE Industries, Ltd.

Membrane 22, probe bumps 24, and conductors 28 comprise what will be referred to as a membrane test head or a membrane probe. Probe bumps 24 and conductors 28 are formed using conventional printed circuit board techniques on a top surface of membrane 22. Alternatively, conductors 28 may be formed on a bottom surface while probe bumps 24 are on the top surface. In this case, conductors 28 must be coupled to probe bumps 24 by vias formed in membrane 22. Probe bumps 24 are sized so that they can couple to leads 13 as will be described in greater detail hereinafter. Conductive lines 28 couple probe bumps 24 to an edge of membrane 22. Tester 27 is coupled to conductive lines 28 at the edge of membrane 22 as it is conventionally done between testers and printed circuit boards. One probe bump 24/conductive line 28 pair is supplied for each lead 13 of package 12 to be tested.

Since conductors 28 and probe bumps 24 are formed with conventional printed circuit board techniques, it should be apparent that the membrane test head has a great deal of layout flexibility. The membrane test head can be adapted to various device types and leadframe orientations by simply changing the layout of probe bumps 24 and conductors 28 on the surface of membrane 22. It is desirable to form conductive lines 28 so that they are microstrip transmission lines to improve the quality of signals transmitted from the tester to the integrated circuit.

Package 12 is shown after leads 13 have been mechanically separated from each other and leadframe 11'. Leads 13 have been spanked down at an angle which is a first step in the leadform process. Before the leadform process is completed, leads 13 are aligned to probe bumps 24 as shown. Tie-bars 14 (see FIG.1) still couple package 12 to leadframe 11'. Supports 26 have a track which holds leadframe 11' in place during the trim, test, and leadform processes and allow the leadform to be indexed from one stage to the next. Because the location of package 12 is fixed with respect to leadframe 11', as are the locations of leads 13, alignment is easily accomplished when leadframe 11' is indexed into position over the membrane test head.

Once leads 13 are aligned to probe bumps 24, bladder 23 is inflated which in turn presses probe bumps 24 against leads 13. In this manner, contact is made between leads 13 and the tester. Power, ground, and test signals can be applied to leads 13 to evaluate the functionality of the integrated circuit inside package 12. Usually, leadframe 11' and tie bars 14 are coupled to the substrate of the integrated circuit inside package 12, therefore it may be necessary to provide a power or ground connection to leadframe 11' during testing. It should be noted also that several packages 12 be tested simultaneously in this manner by making bladder 23 into a long cigar-shaped bladder, and extending membrane 22 having a plurality of probe bumps 24, as shown in FIG. 4, along the length of bladder 23. When this is done, a plurality of integrated circuits can be tested simultaneously, greatly improving test cycle time.

After the circuit inside package 12 has been tested, it is desirable to record the pass/fail information for each package 12 in order to separate good from bad devices once the packages are singulated. Once testing is complete, bladder 23 is deflated to decouple probe bumps 24 from leads 13. Leadframe 11' is indexed to a portion of the trim and leadform tool which completes the leadforming. Once this is complete, tie-bars 14, shown in FIG. 1, are trimmed thus singulating packages 12 Now, circuits which have passed the test are separated from those which have failed the test using the recorded pass/fail information.

By now, it should be appreciated that a method of testing integrated circuits is provided which greatly improves the cycle time of the test operation by allowing parallel testing, and by testing in line with a trim and leadform process. Also, the testing method provided greatly reduces package defects and leadform damage during testing as the packages are firmly held in the leadframe during testing, and the leadform is completed after testing.

I claim:

1. A method of testing a plurality of integrated circuits which are enclosed in packages, wherein the packages are attached to a leadframe and a number of leads which are coupled to each of the integrated circuits extend from each package, the method comprising the steps of: separating the leads from each other and from the leadframe; coupling a tester to the leads; testing the integrated circuits; and separating the packages from the leadframe after testing.

2. The method of claim 1 further comprising the step of bending the leads away from the package after the step of separating the leads from each other and the leadframe; and moving test contacts to the leads in order to perform the coupling.

3. The method of claim 2 further comprising the step of bending the leads into a predefined shape after testing the integrated circuits and before separating the packages from the leadframe.

4. A test fixture for testing a plurality of packaged integrated circuits which are attached to a leadframe, wherein each of the integrated circuits has a plurality of leads which are isolated from the leadframe, the test fixture comprising:

a membrane test head having a plurality of contacts thereon positioned underneath the plurality of leads;

a tester coupled to the test head;

a drive means for moving the test head towards and away from the plurality of leads, wherein the membrane test head couples to a plurality of packaged ICs at one time.

5. The test fixture of claim 4 wherein the plurality of ICs are tested in parallel.

6. The test fixture of claim 4 wherein the ICs are tested serially by multiplexing the tester to each IC of the plurality of ICs.

7. A method for leadforming and testing a plurality of integrated circuits in individual packages, wherein the packages are attached to a leadframe by tie bars and a number of leads which are coupled to the integrated circuits, the method comprising: cutting the leads and the bars to electrically separate the number of leads from each other and from the leadframe; bending the leads so that a portion of each of the leads extends below the package; contacting the leads with a membrane test head located below the packages, the membrane test head having a number of probe bumps which are coupled to an external tester and which are aligned to the number of leads of the plurality of integrated circuits; an innflatable bladder located below the membrane test head; bending the leads to complete a leadform; and cutting the tie bars to separate the package from the leadframe.

8. The method of claim 7 further comprising providing a number of microstrip transmission lines formed on the membrane test head, wherein each microstrip transmission line is coupled to a probe bump and to the tester.

9. The method of claim 7 further comprising filling the inflatable bladder with gas to move the membrane test head so that the probe bumps couple to the leads.

* * * * *

Exhibit C

US005081454A

United States Patent [19]

Campbell, Jr. et al.

[11] Patent Number: 5,081,454

[45] Date of Patent: Jan. 14, 1992

[54] **AUTOMATIC A/D CONVERTER OPERATION USING PROGRAMMABLE SAMPLE TIME**

[75] Inventors: **Jules D. Campbell, Jr.; William D. Huston; Mark R. Heene**, all of Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **577,222**

[22] Filed: **Sep. 4, 1990**

[51] **Int. Cl.**[5] **H03M 1/12**

[52] **U.S. Cl.** **341/141**; 341/155

[58] **Field of Search** 341/122, 141, 155

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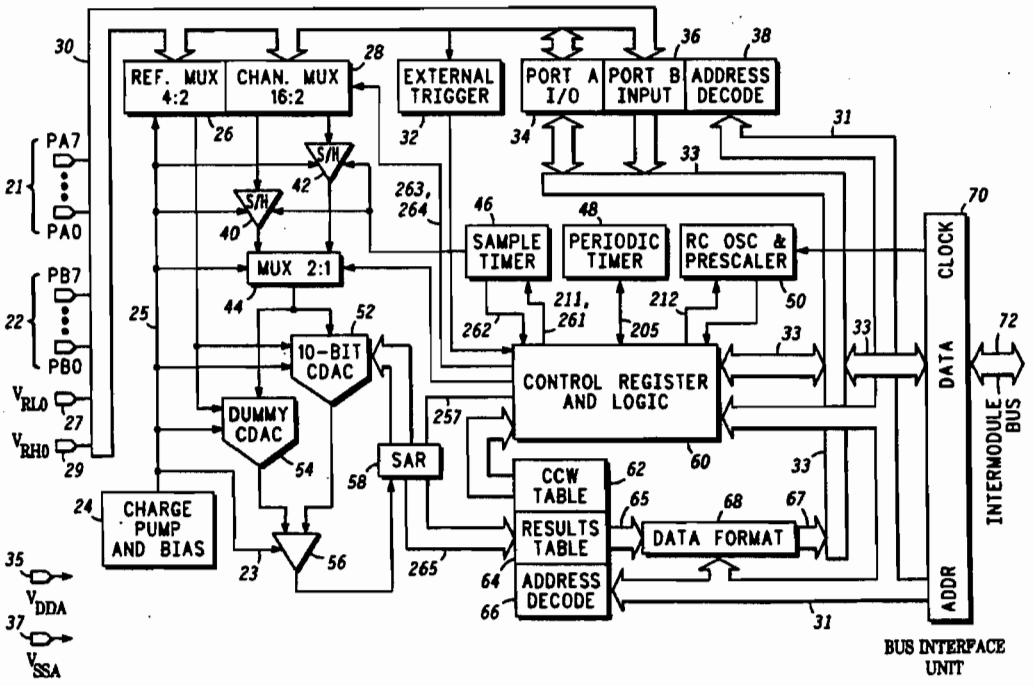
Primary Examiner—A. D. Pellinen
Assistant Examiner—Marc S. Hoff
Attorney, Agent, or Firm—Walt Nielsen; Jonathan P. Meyer

[57] **ABSTRACT**

An analog-to-digital conversion system module and method provides programmable times for sampling analog input signals. Software involvement is minimized by providing a command word which includes information specifying a sample time. The command word may be stored in a register or memory table. The command word or words may specify the conversion time per analog input channel or group of channels, and per conversion or conversion sequence. In one embodiment a control table comprises a plurality of conversion command words (CCW's). Each CCW designates conversion parameters including the input sample time.

27 Claims, 14 Drawing Sheets



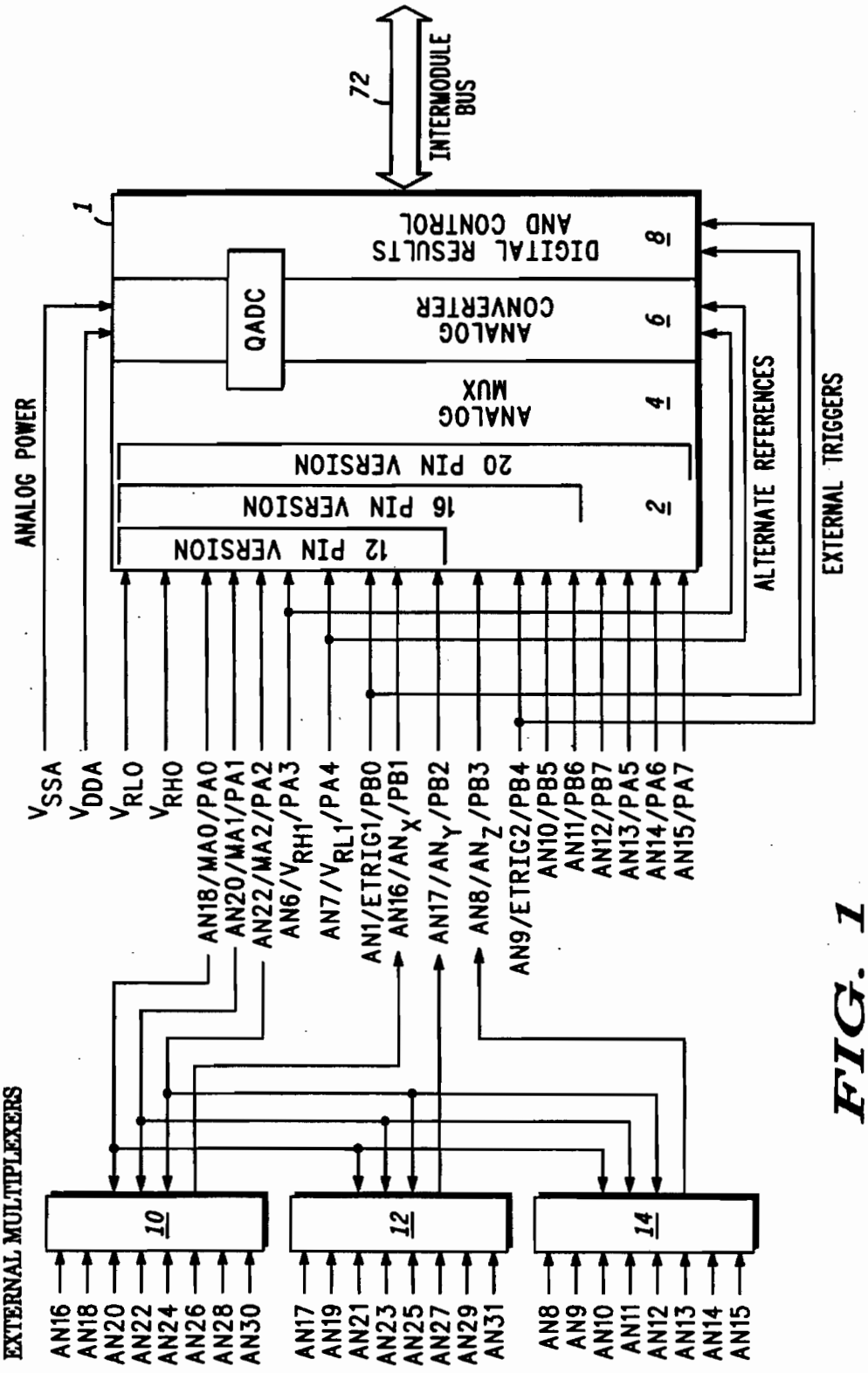
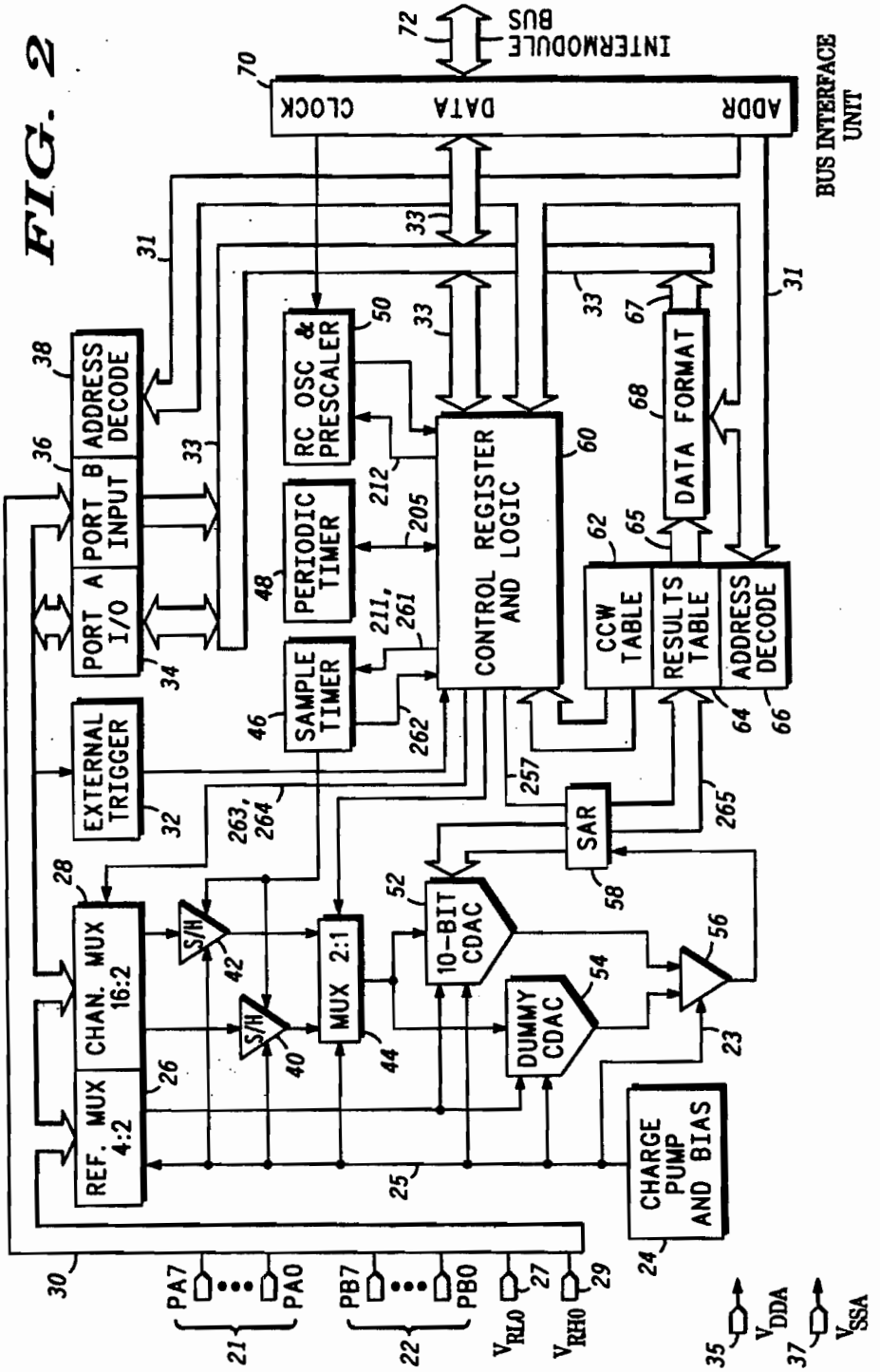

72
INTERMODULE BUS
1
DIGITAL RESULTS AND CONTROL
8
QADC
ANALOG CONVERTER
6
ANALOG MUX
4
20 PIN VERSION
16 PIN VERSION
12 PIN VERSION
2
ANALOG POWER
ALTERNATE REFERENCES
EXTERNAL TRIGGERS
VSSA
VDDA
VRLO
VRHO
AN18/MA0/PA0
AN20/MA1/PA1
AN22/MA2/PA2
AN6/VRH1/PA3
AN7/VRL1/PA4
AN1/ETRIG1/PB0
AN16/ANX/PB1
AN17/ANY/PB2
AN8/ANZ/PB3
AN9/ETRIG2/PB4
AN10/PB5
AN11/PB6
AN12/PB7
AN13/PA5
AN14/PA6
AN15/PA7
EXTERNAL MULTIPLEXERS
10
12
14
AN16 AN18 AN20 AN22 AN24 AN26 AN28 AN30
AN17 AN19 AN21 AN23 AN25 AN27 AN29 AN31
AN8 AN9 AN10 AN11 AN12 AN13 AN14 AN15

FIG. 1

FIG. 2


INTERMODULE BUS
ADDR
DATA
CLOCK
BUS INTERFACE UNIT
ADDRESS DECODE
PORT B INPUT
PORT A I/O
RC OSC & PRESCALER
PERIODIC TIMER
SAMPLE TIMER
EXTERNAL TRIGGER
CONTROL REGISTER AND LOGIC
DATA FORMAT
CCW TABLE
RESULTS TABLE
ADDRESS DECODE
SAR
10-BIT CDAC
DUMMY CDAC
CHAN. MUX 16:2
REF. MUX 4:2
MUX 2:1
S/H
CHARGE PUMP AND BIAS
PA7
PA0
PB7
PB0
V_{RLO}
V_{RHO}
V_{DDA}
V_{SSA}

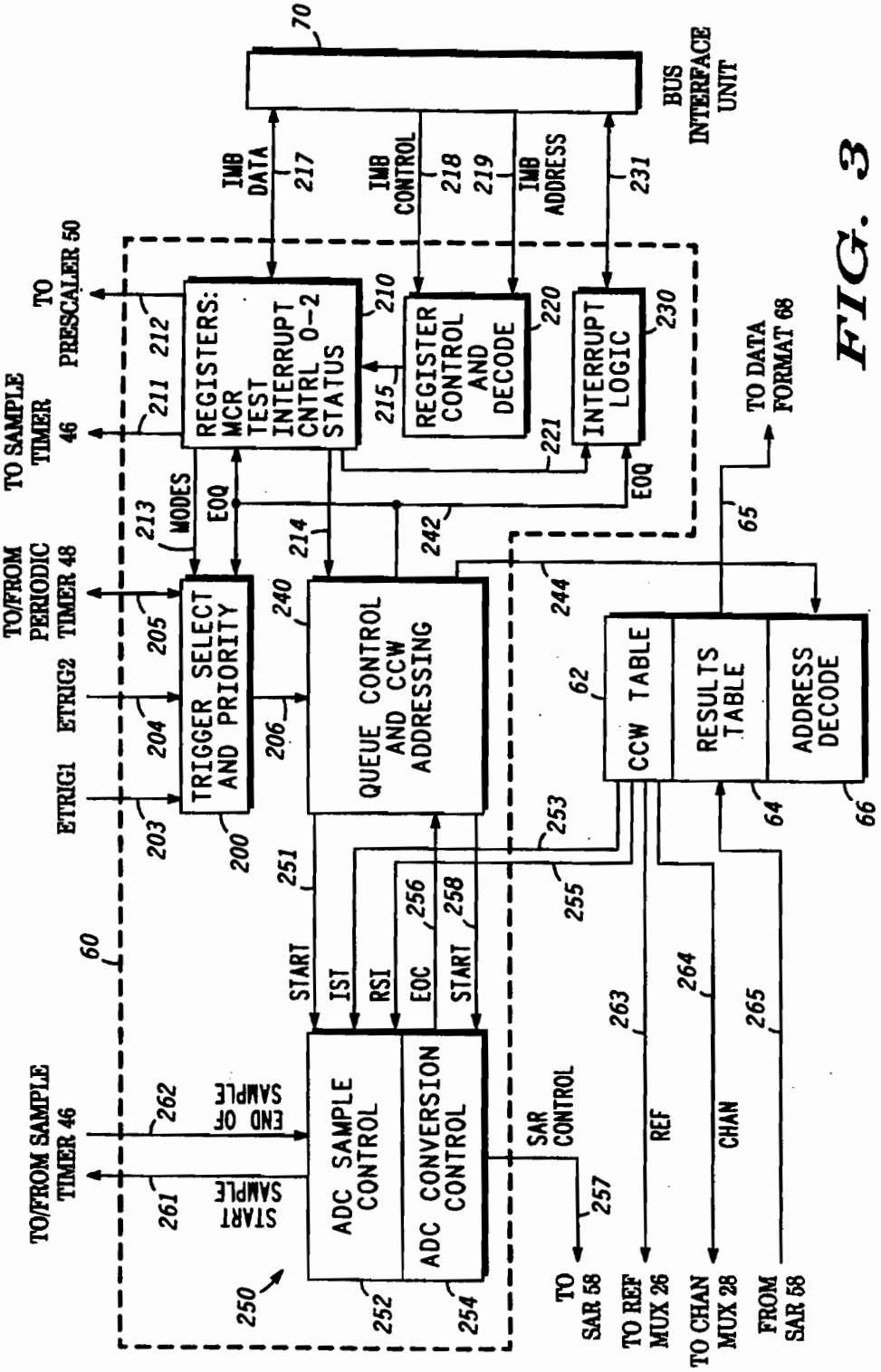
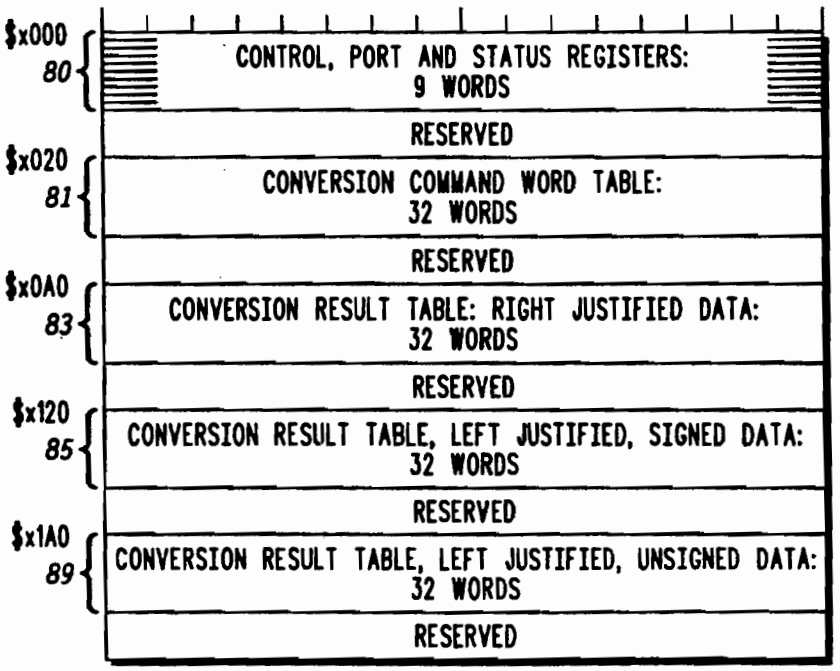

70
BUS INTERFACE UNIT
IMB DATA
IMB CONTROL
IMB ADDRESS
217
218
219
231
TO PRESCALER 50
TO SAMPLE TIMER 46
TO/FROM PERIODIC TIMER 48
ETRIG2
ETRIG1
REGISTERS: MCR TEST INTERRUPT CNTRL 0-2 STATUS
REGISTER CONTROL AND DECODE
INTERRUPT LOGIC
TO DATA FORMAT 68
MODES
EOQ
TRIGGER SELECT AND PRIORITY
QUEUE CONTROL AND CCW ADDRESSING
CCW TABLE
RESULTS TABLE
ADDRESS DECODE
START
IST
RSI
EOC
START
ADC SAMPLE CONTROL
ADC CONVERSION CONTROL
SAR CONTROL
TO/FROM SAMPLE TIMER 46
END OF SAMPLE
START SAMPLE
TO SAR 58
TO REF MUX 26
TO CHAN MUX 28
FROM SAR 58
REF
CHAN

FIG. 3

SIGNAL NAME	MNEMONIC	IMB I/O
SYSTEM CLOCK	ICLOCK	INPUT FROM IMB
MASTER RESET	IMSTRSTB	INPUT FROM IMB
SYSTEM RESET	ISYSRSTB	INPUT FROM IMB
FREEZE	IFREEZEB	INPUT FROM IMB
TEST	ITSTMODB	INPUT FROM IMB
INTERNAL PERIPHERAL SELECT	IIPCSB	INPUT FROM IMB
MODULE MAPPING	IMODMAP	INPUT FROM IMB
FUNCTION CODES	IFC[3:0]	INPUT FROM IMB
CYCLE START	ICYSB	INPUT FROM IMB
WRITE	IWRITEB	INPUT FROM IMB
ADDRESS BUS	IADDR[23:0]	INPUT FROM IMB
ADDRESS STROBE	IASB	INPUT FROM IMB
ADDRESS ACKNOWLEDGE	IAACKB	OUTPUT TO IMB
SIZE	ISIZ[1:0]	INPUT FROM IMB
DATA STROBE	IDSB	INPUT FROM IMB
DATA BUS	IDATA[15:0]	INPUT/OUTPUT FROM/TO IMB
DATA TRANSFER ACKNOWLEDGE	IDTACKB	OUTPUT TO IMB
BUS ERROR	IBERRB	OUTPUT TO IMB
INTERRUPT REQUEST LEVEL	IRQ[7:1]	OUTPUT TO IMB
INTERRUPT ARBITRATION	IARB[1:0]	INPUT/OUTPUT FROM/TO IMB

FIG. 4

FIG. 5



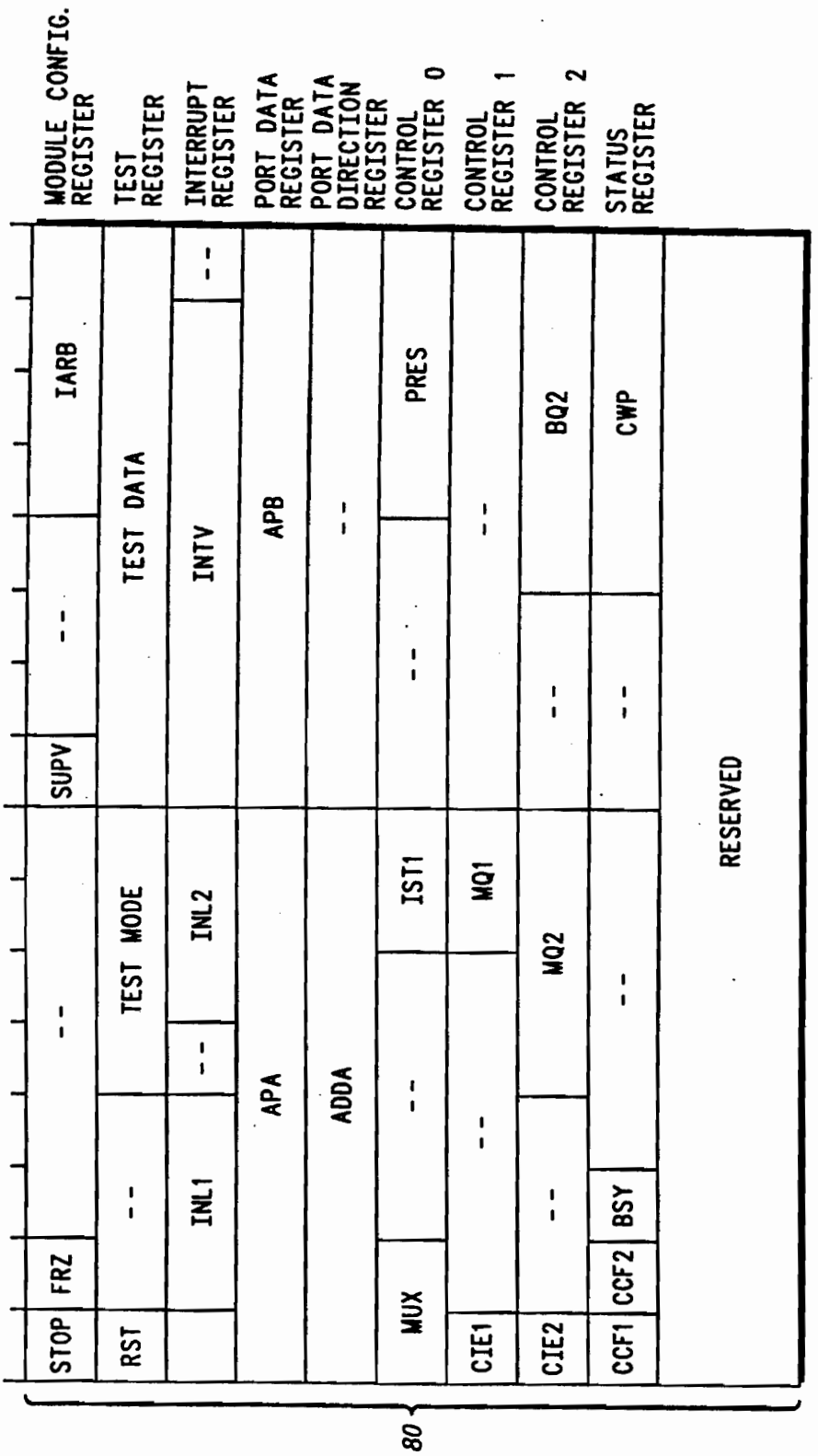

MODULE CONFIG. REGISTER
TEST REGISTER
INTERRUPT REGISTER
PORT DATA REGISTER
PORT DATA DIRECTION REGISTER
CONTROL REGISTER 0
CONTROL REGISTER 1
CONTROL REGISTER 2
STATUS REGISTER
STOP
FRZ
--
SUPV
--
IARB
RST
--
TEST MODE
--
TEST DATA
INL1
--
INL2
--
INTV
--
APA
APB
ADDA
--
MUX
--
IST1
--
PRES
CIE1
--
MQ1
--
CIE2
--
MQ2
--
BQ2
CCF1
CCF2
BSY
--
CWP
RESERVED
80

FIG. 6

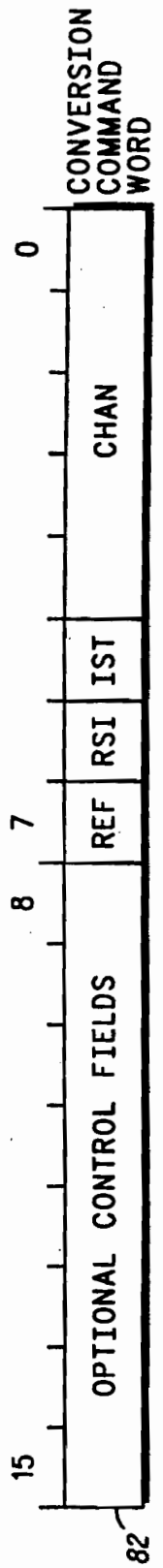


FIG. 7

FIG. 10

NUMBER OF INTERNALLY + EXTERNALLY MUXED ANALOG CHANNELS				
TOTAL PINS AVAILABLE TO QADC MODULE	WITH NO EXTERNAL MUX CHIPS	WITH 1 EXTERNAL MUX CHIP	WITH 2 EXTERNAL MUX CHIPS	WITH 3 EXTERNAL MUX CHIPS
12	8	4 + 8 = 12	3 + 16 = 19	---
14	10	6 + 8 = 14	5 + 16 = 21	3 + 24 = 27
16	12	8 + 8 = 16	7 + 16 = 23	3 + 24 = 27
18	14	10 + 8 = 18	9 + 16 = 25	3 + 24 = 27
20	16	12 + 8 = 20	11 + 16 = 27	3 + 24 = 27

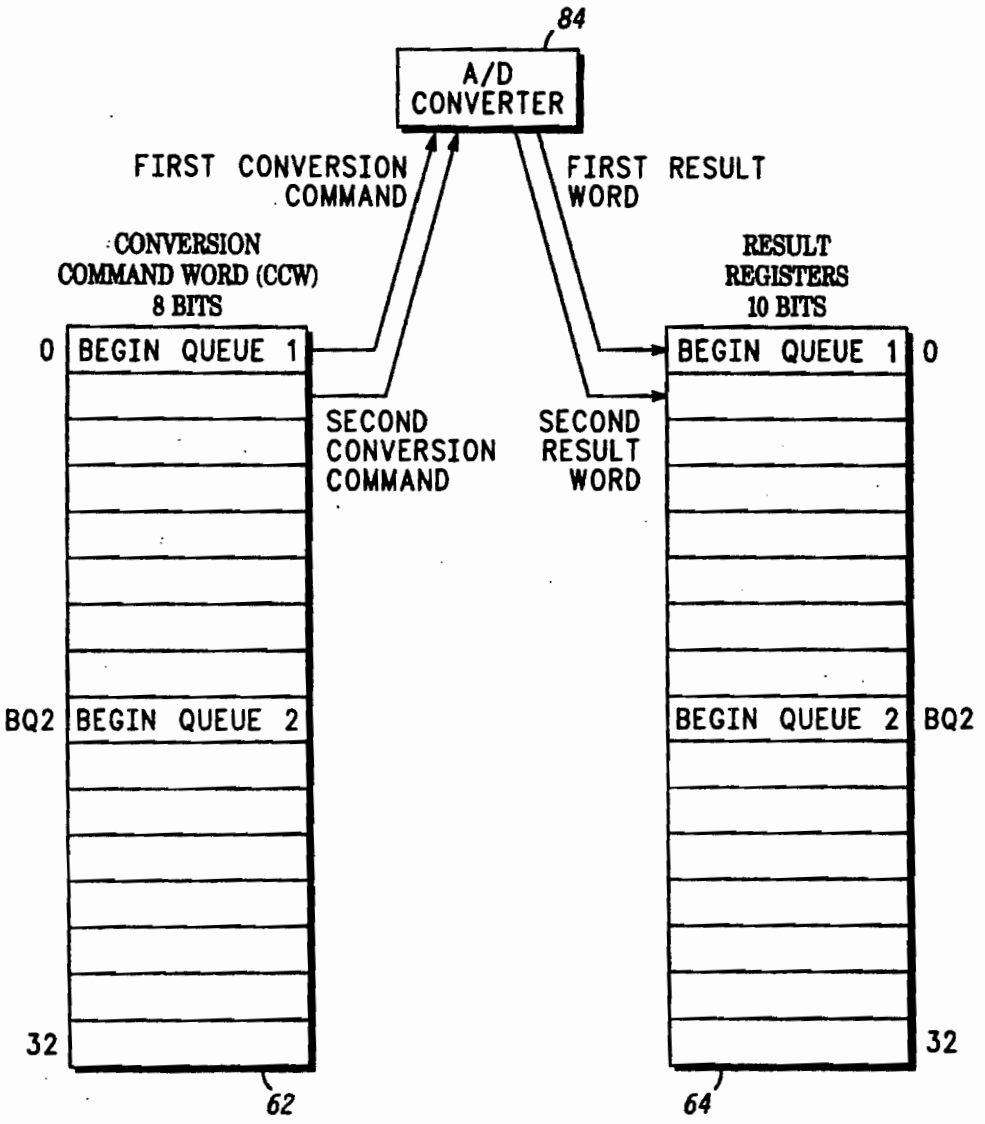

84
A/D CONVERTER
FIRST CONVERSION COMMAND
FIRST RESULT WORD
CONVERSION COMMAND WORD (CCW) 8 BITS
RESULT REGISTERS 10 BITS
0
BEGIN QUEUE 1
SECOND CONVERSION COMMAND
SECOND RESULT WORD
BQ2
BEGIN QUEUE 2
32
62
64

FIG. 8

CCW CHAN BITS	MUX=00 INT.MUX CHANNEL SELECTED	MUX=01 EXT.MUX CHANNEL SELECTED	MUX=10 EXT.MUX CHANNEL SELECTED	MUX=11 EXT.MUX CHANNEL SELECTED
00000	END OF QUEUE	END OF QUEUE	END OF QUEUE	END OF QUEUE
00001	ETRIG1/AN1	ETRIG1/AN1	ETRIG1/AN1	ETRIG1/AN1
00010	$(V_{RH0}-V_{RL0})\div 2$	$(V_{RH0}-V_{RL0})\div 2$	$(V_{RH0}-V_{RL0})\div 2$	$(V_{RH0}-V_{RL0})\div 2$
00011	$(V_{RH1}-V_{RL1})\div 2$	$(V_{RH1}-V_{RL1})\div 2$	$(V_{RH1}-V_{RL1})\div 2$	$(V_{RH1}-V_{RL1})\div 2$
00100	V_{SSA}/V_{RL0}	V_{SSA}/V_{RL0}	V_{SSA}/V_{RL0}	V_{SSA}/V_{RL0}
00101	V_{DDA}/V_{RH0}	V_{DDA}/V_{RH0}	V_{DDA}/V_{RH0}	V_{DDA}/V_{RH0}
00110	$AN6/V_{RL1}$	$AN6/V_{RL1}$	$AN6/V_{RL1}$	$AN6/V_{RL1}$
00111	$AN7/V_{RH1}$	$AN7/V_{RH1}$	$AN7/V_{RH1}$	$AN7/V_{RH1}$
01000	AN8	AN8	AN8	AN_Z
01001	ETRIG2/AN9	ETRIG2/AN9	ETRIG2/AN9	AN_Z
01010	AN10	AN10	AN10	AN_Z
01011	AN11	AN11	AN11	AN_Z
01100	AN12	AN12	AN12	AN_Z
01101	AN13	AN13	AN13	AN_Z
01110	AN14	AN14	AN14	AN_Z
01111	AN15	AN15	AN15	AN_Z
10000	AN16	AN_X	AN_X	AN_X
10001	AN17	AN17	AN_Y	AN_Y
10010	AN18	AN_X	AN_X	AN_X
10011	UNUSED	UNUSED	AN_Y	AN_Y
10100	AN20	AN_X	AN_X	AN_X
10101	UNUSED	UNUSED	AN_Y	AN_Y
10110	AN22	AN_X	AN_X	AN_X
10111	UNUSED	UNUSED	AN_Y	AN_Y
11000	UNUSED	AN_X	AN_X	AN_X
11001	UNUSED	UNUSED	AN_Y	AN_Y
11010	UNUSED	AN_X	AN_X	AN_X
11011	UNUSED	UNUSED	AN_Y	AN_Y
11100	UNUSED	AN_X	AN_X	AN_X
11101	UNUSED	UNUSED	AN_Y	AN_Y
11110	UNUSED	AN_X	AN_X	AN_X
11111	UNUSED	UNUSED	AN_Y	AN_Y

FIG. 9

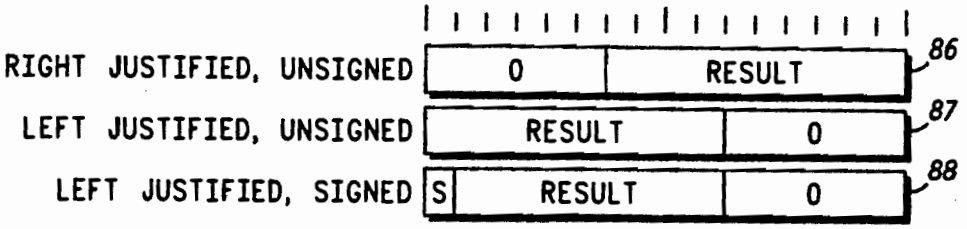


FIG. 11

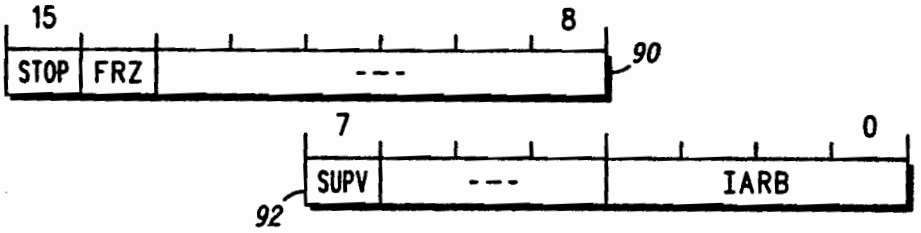
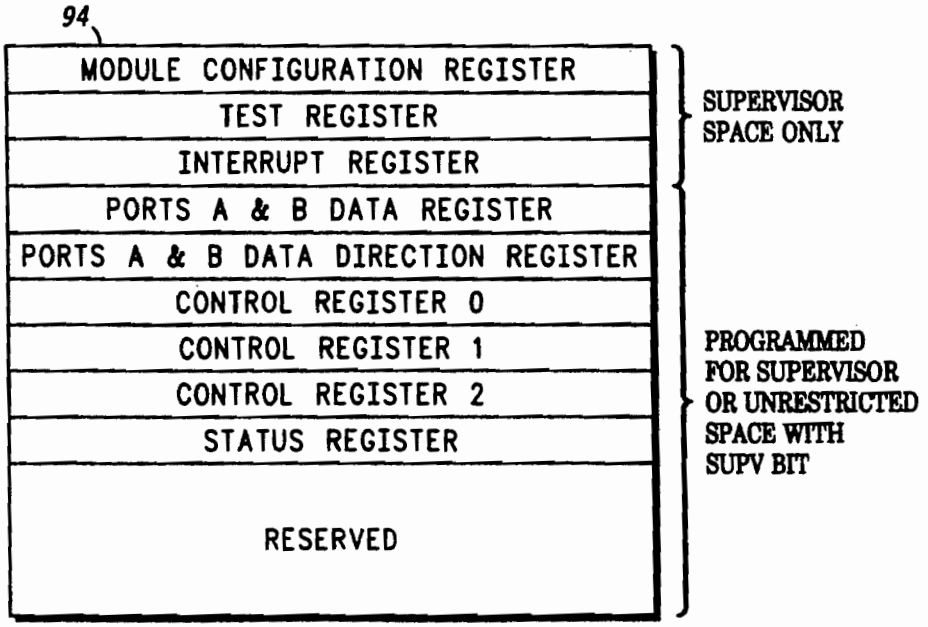


FIG. 12

FIG. 13



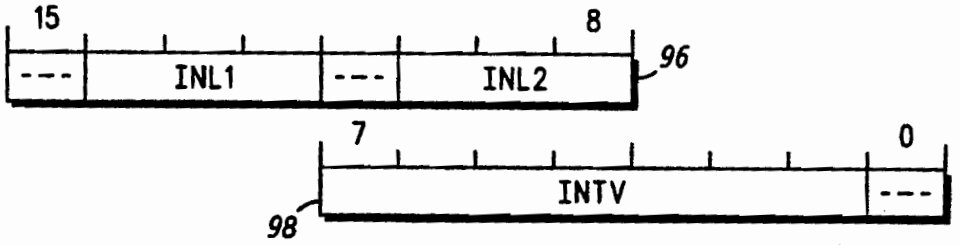


FIG. 14

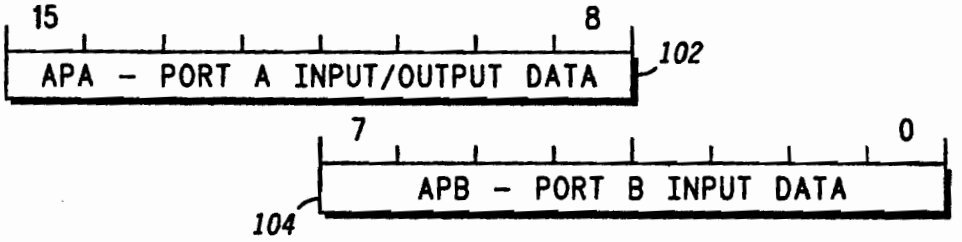


FIG. 15

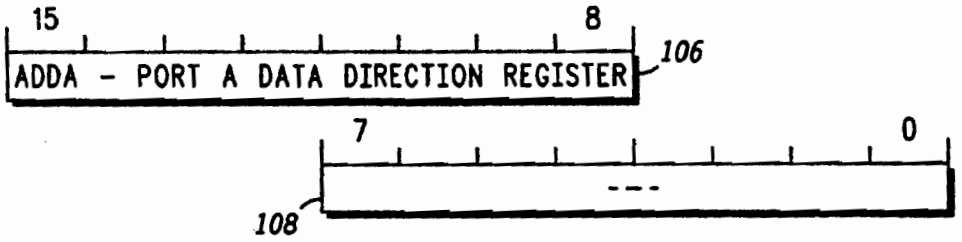


FIG. 16

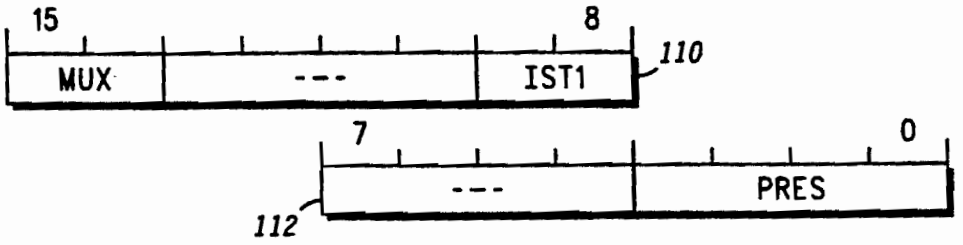


FIG. 17

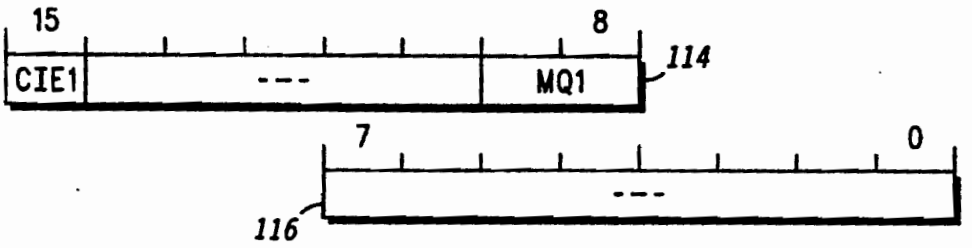


FIG. 18

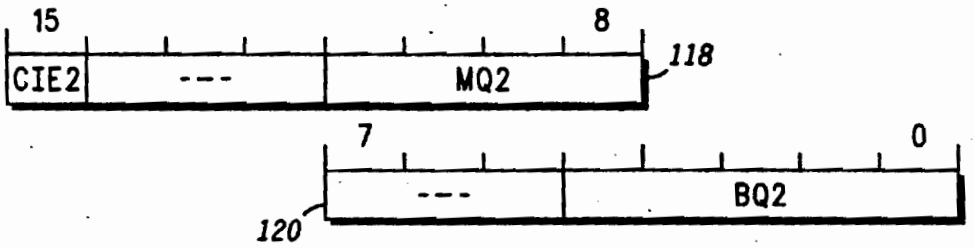


FIG. 19

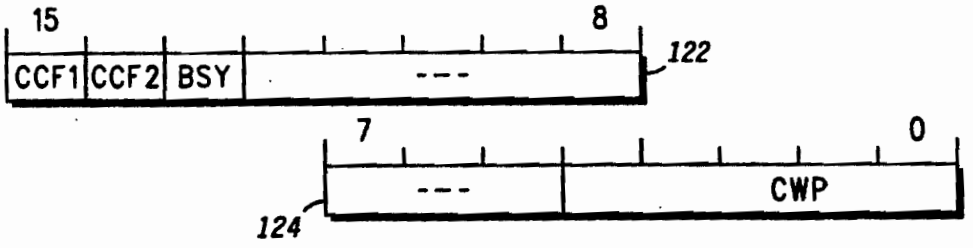


FIG. 20

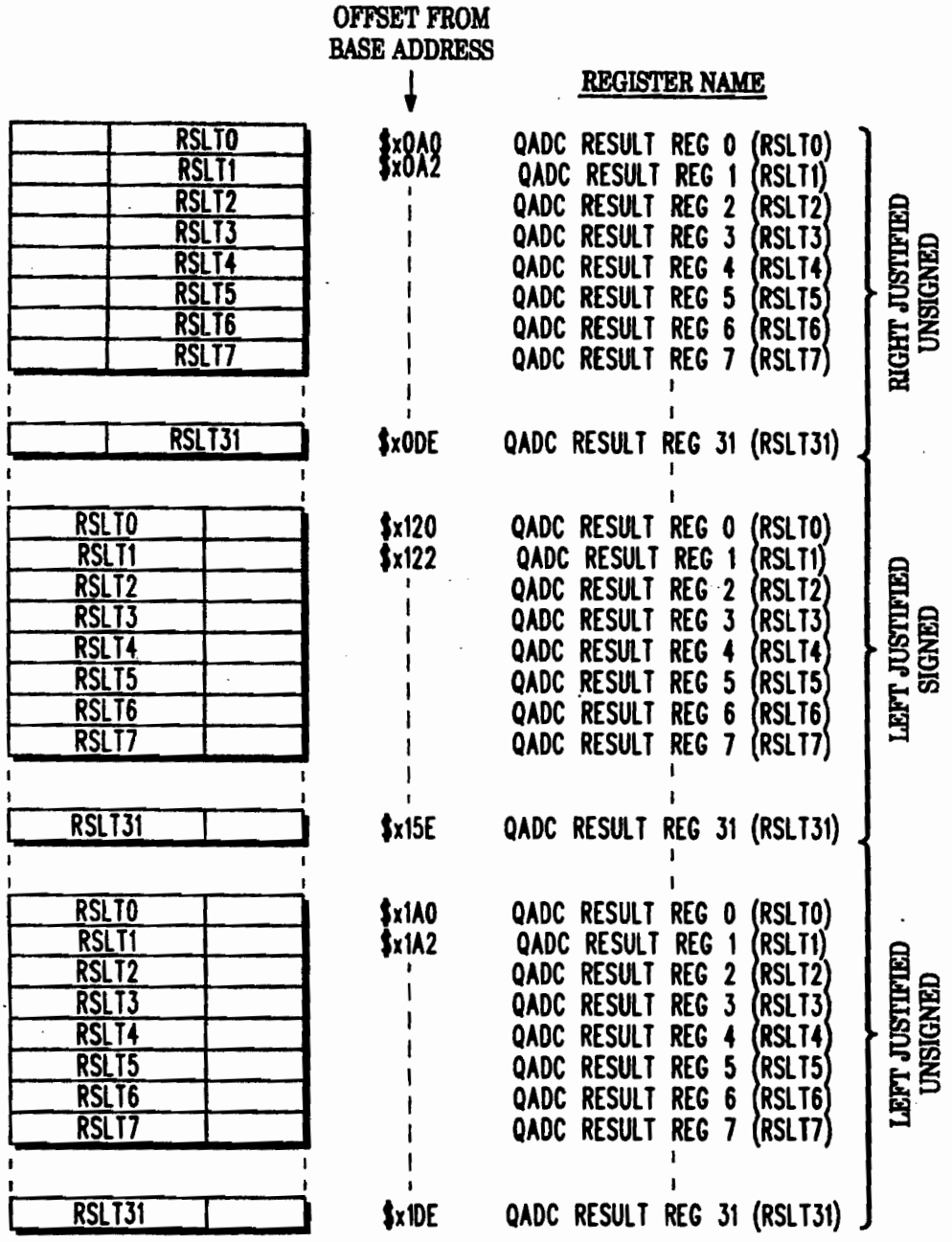
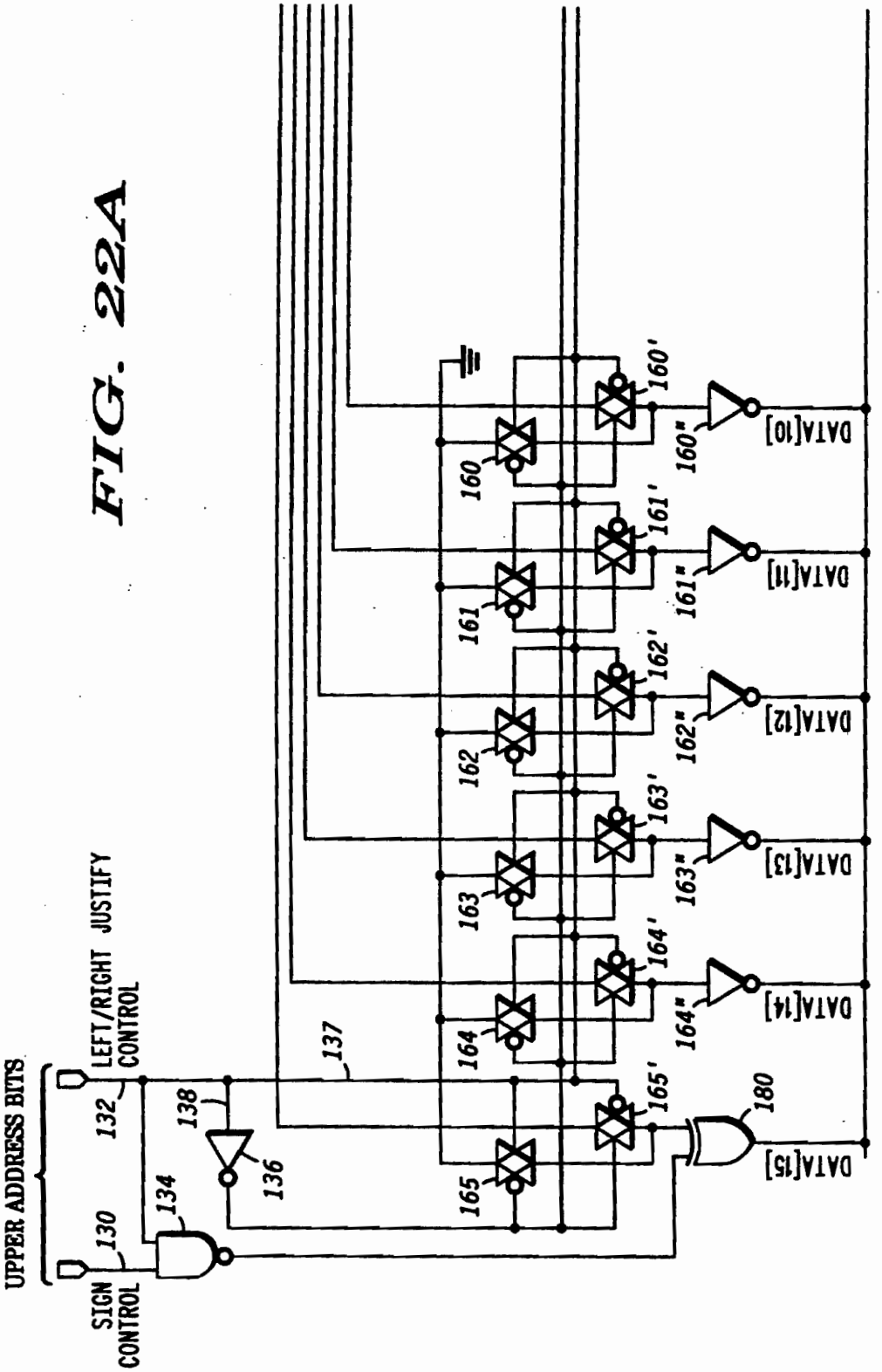

OFFSET FROM BASE ADDRESS
REGISTER NAME
RSLT0
RSLT1
RSLT2
RSLT3
RSLT4
RSLT5
RSLT6
RSLT7
RSLT31
$x0A0 QADC RESULT REG 0 (RSLT0)
$x0A2 QADC RESULT REG 1 (RSLT1)
QADC RESULT REG 2 (RSLT2)
QADC RESULT REG 3 (RSLT3)
QADC RESULT REG 4 (RSLT4)
QADC RESULT REG 5 (RSLT5)
QADC RESULT REG 6 (RSLT6)
QADC RESULT REG 7 (RSLT7)
$x0DE QADC RESULT REG 31 (RSLT31)
RIGHT JUSTIFIED UNSIGNED
$x120 QADC RESULT REG 0 (RSLT0)
$x122 QADC RESULT REG 1 (RSLT1)
QADC RESULT REG 2 (RSLT2)
QADC RESULT REG 3 (RSLT3)
QADC RESULT REG 4 (RSLT4)
QADC RESULT REG 5 (RSLT5)
QADC RESULT REG 6 (RSLT6)
QADC RESULT REG 7 (RSLT7)
$x15E QADC RESULT REG 31 (RSLT31)
LEFT JUSTIFIED SIGNED
$x1A0 QADC RESULT REG 0 (RSLT0)
$x1A2 QADC RESULT REG 1 (RSLT1)
QADC RESULT REG 2 (RSLT2)
QADC RESULT REG 3 (RSLT3)
QADC RESULT REG 4 (RSLT4)
QADC RESULT REG 5 (RSLT5)
QADC RESULT REG 6 (RSLT6)
QADC RESULT REG 7 (RSLT7)
$x1DE QADC RESULT REG 31 (RSLT31)
LEFT JUSTIFIED UNSIGNED

FIG. 21

FIG. 22A


UPPER ADDRESS BITS
SIGN CONTROL
LEFT/RIGHT JUSTIFY CONTROL
130
132
134
136
137
138
160
160'
160"
161
161'
161"
162
162'
162"
163
163'
163"
164
164'
164"
165
165'
180
DATA[10]
DATA[11]
DATA[12]
DATA[13]
DATA[14]
DATA[15]

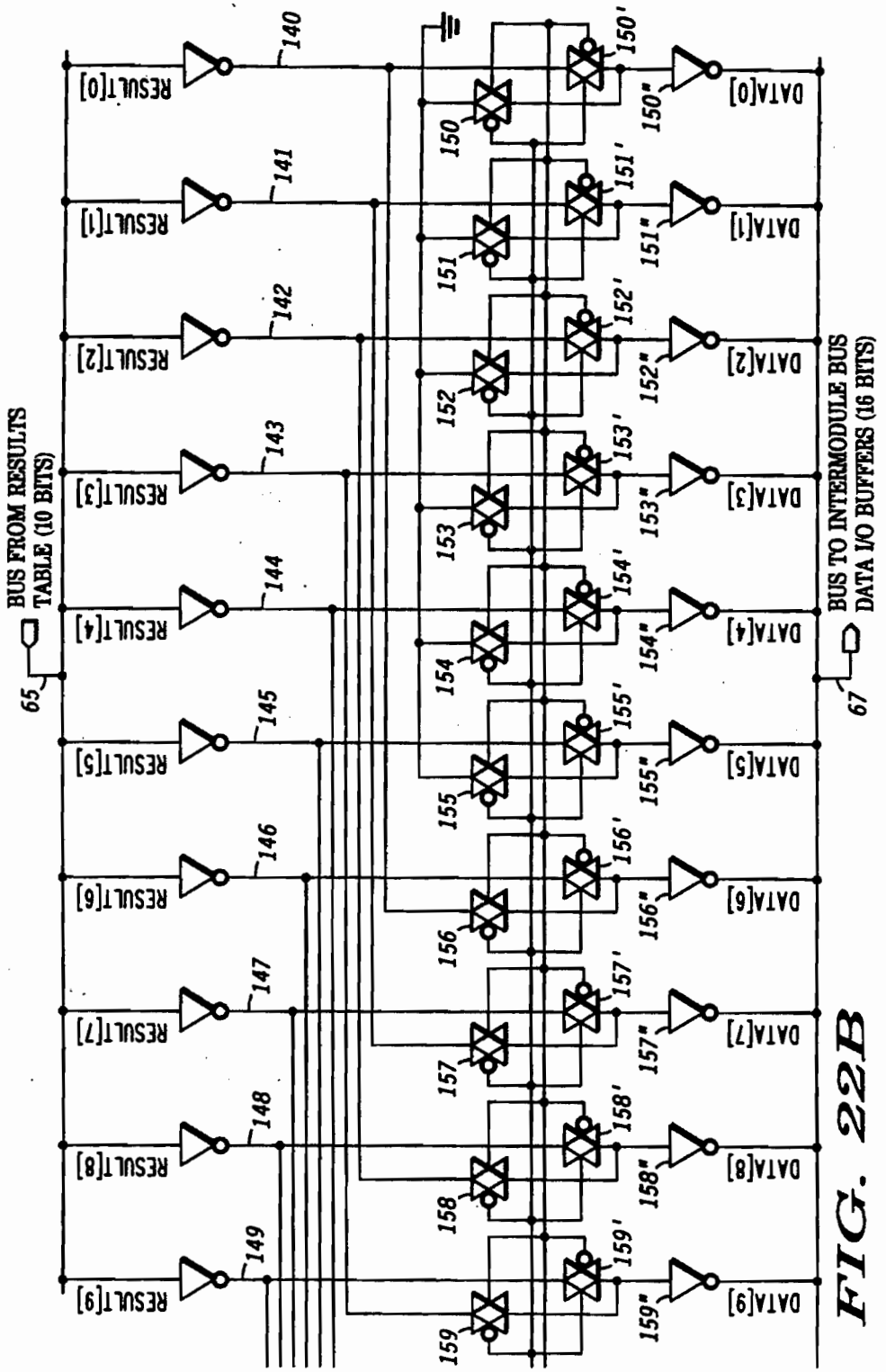

BUS FROM RESULTS TABLE (10 BITS)
65
RESULT[0]
RESULT[1]
RESULT[2]
RESULT[3]
RESULT[4]
RESULT[5]
RESULT[6]
RESULT[7]
RESULT[8]
RESULT[9]
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
150'
151'
152'
153'
154'
155'
156'
157'
158'
159'
150"
151"
152"
153"
154"
155"
156"
157"
158"
159"
DATA[0]
DATA[1]
DATA[2]
DATA[3]
DATA[4]
DATA[5]
DATA[6]
DATA[7]
DATA[8]
DATA[9]
BUS TO INTERMODULE BUS DATA I/O BUFFERS (16 BITS)
67

FIG. 22B

AUTOMATIC A/D CONVERTER OPERATION USING PROGRAMMABLE SAMPLE TIME

RELATED INVENTIONS

1. Automatic Selection of External Multiplexer Channels By A/D Converter Integrated Circuit, invented by Jules D. Campbell, Jr. et al., U.S. Ser. No. 07/577,249, filed concurrently herewith and assigned to the assignee of the present invention.

2. Automatic A/D Converter Operation Using A Programmable Control Table, invented by William D. Huston et al., U.S. Ser. No. 07/577,223, filed concurrently herewith and assigned to the assignee of the present invention.

3. Automatic A/D Converter Operation With Selectable Result Format, invented by Jules D. Campbell, Jr. et al., U.S. Ser. No. 07/577,247, filed concurrently herewith and assigned to the assignee of the present invention.

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to analog-to-digital converters, and, more particularly, to an A/D converter system which provides programmable times for sampling analog signals.

BACKGROUND INFORMATION

The present invention has utility in applications requiring the conversion of an analog signal into a digital signal, for example for computer sensing of analog information in an automotive control system. To further illustrate, in an automotive engine control system, a microcomputer requires analog signal information from various transducers to be converted into digital signal information before it can be processed by the microcomputer. Examples of such analog signal information are the outputs of sensors for manifold pressure, oxygen, rotational speed, operator input, battery voltage, anti-knock, etc.

In a typical automotive application, many different analog signals need to be converted. The analog signals originate from many different sources and typically have different source impedances.

Most known A/D converter systems have a fixed input sample time which is determined by the hardware design of the system. The sample time should be some multiple (such as 10) of the "RC" time constant to ensure sampling to the desired accuracy. In an unbuffered charge distribution A/D converter system, a fixed sample time places restrictions on either the conversion time or the source impedance.

In prior art A/D converter systems, high impedance sources often require amplifying or long sample times, which could be adversely affected by rapidly changing signals. Long sample times also restrict the number of samples per second that can be converted. Short sample times require low source impedances, which constrain the driving circuitry.

A known A/D converter system (TI TMS370 available from Texas Instruments Corp.) utilizes software control bits by which processor software initiates sampling and then the software initiates conversion a measured time later. This is unduly burdensome on the host system software.

Thus there is a significant need to provide an A/D converter system with a variable sample time in which the host system software is freed from the responsibility

of initiating the sampling operation and later the conversion operation.

BRIEF SUMMARY OF INVENTION

The present invention fulfills the above-mentioned requirement by providing an A/D converter system and method in which a sampling operation on each of a plurality of analog channels may be initiated automatically by the A/D converter module, and a conversion operation is subsequently initiated, without involving the main system CPU. It should be understood that the term "module" is used herein to indicate either an integrated circuit or a portion of an integrated circuit.

In a preferred embodiment, the A/D converter module is provided with means for storing information regarding sample time. The storage means may be implemented in a number of different ways, taking the form, for example, of a single register, multiple registers, a table in memory, etc.

In a preferred embodiment the sample period information is stored in one or more automatic conversion sequences or queues. Each queue specifies a sequence of sampling operations on one or more channels.

A queue comprises a table of Conversion Command Words (CCW's) stored in memory, located either in the A/D converter or in the CPU address space. Regarding the present invention, each CCW contains an input sample time field (IST); in addition, other fields are provided to control such parameters as analog channel, reference selection, conversion resolution, result data justification, and so on.

In general, the host system software programs the characteristics of the queued operation during a software initialization sequence. Thereafter, the queues execute autonomously, depending upon the external system or internal module events which have been programmed to initiate the conversion sequences.

One or more bits in the CCW and/or in a control register can be pre-programmed to vary the input sample time. The sample time can be varied in numerous ways—e.g. per channel or group of channels, per conversion, per conversion scan, and so forth.

Programmable sample time allows operation without a loss of accuracy and a higher overall conversion throughput. It is particularly useful for applications with widely varying source impedances.

The A/D converter can issue an interrupt when the conversion scan sequence is complete, allowing the host system software to read the results.

Thus the present invention frees the host system software from the responsibility of initiating the sample and conversion operations of the A/D converter.

The present invention also allows the flexibility of working with a range of source impedances and a charge-redistribution capacitive D/A converter. The invention enables operation with higher source impedances without a loss of accuracy.

Accordingly, it is an object of the present invention to provide an A/D converter system and method which control the duration of the sampling of analog inputs while minimizing the involvement of host system software.

It is another object of the present invention to provide an A/D converter system and method in which parameters for controlling the input sample times are initially loaded into a table or register, and thereafter the A/D conversion system autonomously carries out

the desired sampling and conversion without further involvement of host system software.

These and other objects are achieved in accordance with a preferred embodiment of the invention by providing an analog-to-digital conversion system comprising an analog-to-digital converter, at least one analog input terminal, means for reading at least one command word, the command word designating an input sample time, means responsive to the reading means for sampling an analog signal on the at least one analog input terminal for the duration of the input sample time; and means responsive to the sampling means for converting the sampled value of the analog signal into a digital value.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is pointed out with particularity in the appended claims. However, other features of the intention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

FIG. 1 shows an A/D converter system, comprising an A/D converter module and one or more multiplexer integrated circuits, in accordance with a preferred embodiment of the present invention.

FIG. 2 shows a block diagram of the A/D converter module of the present invention.

FIG. 3 shows a block diagram of the Control Register and Logic circuit 60 illustrated in FIG. 2.

FIG. 4 defines the Intermodule Bus (IMB) signals of the A/D converter module of the present invention.

FIG. 5 shows an address map for the control registers, Conversion Command Word table, and the Conversion Result Table of the A/D converter module.

FIG. 6 is a more detailed address map showing the formats of the Control, Port, and Status Registers 80 shown in FIG. 5.

FIG. 7 shows the format of a Conversion Command Word (CCW) of the A/D converter module.

FIG. 8 is a conceptual diagram showing how Conversion Command Words are used to produce Result Words which are stored in the Conversion Result Table.

FIG. 9 is a table illustrating how the CCW CHAN bits specify the functions of the various I/O pins for 0, 1, 2, or 3 external multiplexer IC's.

FIG. 10 is a table illustrating the number of analog channels available with different numbers of external multiplexer IC's, in terms of the number of I/O pins allocated to the A/D converter module.

FIG. 11 illustrates the data format options of Result Words stored in the Conversion Result Table.

FIG. 12 shows the format of the Module Configuration Register of the A/D converter module.

FIG. 13 illustrates the use of the SUPV bit of the Module Configuration Register of the A/D converter module.

FIG. 14 shows the format of the Interrupt Register of the A/D converter module.

FIG. 15 shows the formats of the Port A and Port B Data Registers of the A/D converter module.

FIG. 16 shows the format of the Port A Data Direction Register of the A/D converter module.

FIG. 17 shows the format of Control Register 0 of the A/D converter module.

FIG. 18 shows the format of Control Register 1 of the A/D converter module.

FIG. 19 shows the format of Control Register 2 of the A/D converter module.

FIG. 20 shows the format of the Status Register of the A/D converter module.

FIG. 21 illustrates the addresses required to read Result Words stored in the Conversion Result Table in at least three different data format options.

FIGS. 22A and 22B show a detailed logic implementation of the Data Format logic 68 shown in FIG. 2.

DESCRIPTION OF PREFERRED EMBODIMENT

Overview

FIG. 1 shows an A/D converter system, comprising an A/D converter integrated circuit (IC) and one or more multiplexer integrated circuits. A Queued A/D Converter module (QADC) 1 is shown coupled to one or more external multiplexers (MUX's) 10, 12, and 14. In a preferred embodiment QADC 1 and the external MUX's are implemented as integrated circuits. External multiplexers are commercially available from Motorola, Inc., for example, as part numbers MC14051 or MC74HC4051.

The Queued A/D Converter module (QADC) 1 is described herein as "queued", because, as will be described in greater detail below, it operates in response to one or more queues of Conversion Command Words.

QADC 1 comprises a plurality of I/O pins, shown generally by reference numeral 2, an analog MUX portion 4, an analog converter portion 6, and a portion for performing control and storing digital results 8.

The I/O pin configurations of QADC vary from a 12-pin version to an 20-pin version. Also coupled to appropriate pins of QADC 1 are power supplies V_{SSA} and V_{DDA}, references V_{RH0} and V_{RL0}, alternate references V_{RH1} and V_{RL1}, and external triggers ETRIG1 and ETRIG2.

Eight of the I/O pins of QADC 1 function as Port A I/O pins and are labeled PA0–PA7, while eight others function as Port B input pins and are labeled PB0–PB7. The prefix "PA" designates Port A, and the prefix "PB" designates Port B.

The external MUX's 10, 12, and 14 are shown comprising eight analog input channels each. For example, MUX 10 has analog input channels AN16, AN18, AN20, AN22, AN24, AN26, AN28, and AN30.

The external MUX's are addressed via address lines MA0-MA2. The prefix "MA" designates Multiplexed Address. The outputs of MUX's 10, 12, and 14 are coupled to lines ANx, ANy, and ANz, respectively. The prefix "AN" designates Analog Input.

As will be discussed further below, many of the I/O pins 2 are programmable to perform multiple functions.

As will be shown and described below, QADC 1 automatically reads analog signals being input into MUX's 10, 12, and 14 and converts the analog values into digital values which are stored in the digital results portion 8 of QADC 1.

QUEUED A/D CONVERTER MODULE

FIG. 2 shows a block diagram of the A/D converter module of the present invention. The Queued A/D Converter module (QADC) 1 comprises Port A, indicated by reference numeral 21, including pins PA0--PA7, and Port B, indicated by reference numeral 22, including pins PB0–PB7. Ports A and B are coupled to bus 30. A pair of primary reference voltages V_{RL0} 27 and V_{RH0} 29 are also coupled to bus 30.

Also coupled to bus 30 are a Reference MUX (4:2) 26; a Channel MUX (16:2) 28; an External Trigger circuit 32; Port A I/O circuit 34; and Port B input circuit 36. Address Decode circuit 38 is coupled to Port A I/O circuit 34 and Port B input circuit 36.

The Queued A/D Converter module 1 comprises a 10-bit successive approximation converter portion which includes Sample-and-Hold circuits 40 and 42; a 2:1 MUX 44; 10-bit Capacitive Digital-to-Analog Converter (CDAC) (charge redistribution type) 52; Dummy CDAC 54; Comparator 56; and Successive Approximation Register (SAR) 58.

It will be apparent to those of ordinary skill in the art that the successive approximation converter may comprise more or fewer than 10 bits. It will also be apparent that the Digital-to-Analog Converter may be of the resistive-only type, the capacitive-only type, or the resistive/capacitive type.

Charge Pump and Bias circuit 24 provides bias voltages to MUX's 26, 28, and 44, to Sample-and-Hold circuits 40 and 42, to CDAC 52 and Dummy CDAC 54, and to Comparator 56.

The Queued A/D Converter module 1 further comprises a Bus Interface Unit (BIU) 70 coupled to an Intermodule Bus 72. The Intermodule Bus 72, which transmits clock, data, control, and address information bi-directionally, may be coupled to a host data processing system (not shown).

Coupled to Bus Interface Unit 70 via internal address bus 31 are Address Decode circuit 38; Control Register and Logic circuit 60; Data Format circuit 68; and Address Decode circuit 66.

Also coupled to Bus Interface Unit 70 via internal data bus 33 are Port A I/O circuit 34; Port B Input circuit 36; Control Register and Logic circuit 60; and Data Format circuit 68.

Also coupled to Control Register and Logic circuit 60 are External Trigger 32; Sample Timer 46; Periodic Timer 48; Prescaler circuit 50; a random access memory (RAM) storing a table of Command Control Words (CCW's) 62 and a Results Table 64; an Address Decode circuit 66; SAR 58; 2:1 sample and hold MUX 44; and 16:2 Channel MUX 28.

Also coupled to the Queued A/D Converter module 1 are suitable analog power supply voltages via pins VDDA 35 and VSSA 37.

EXTERNAL PINS

In a preferred embodiment, 16 analog channels are provided in the internal multiplexing circuitry of the QADC module 1. The number of channels available externally depends upon package pin availability, and whether external multiplexing is employed. The number of channels in an expanded, externally multiplexed mode is 27 in a preferred embodiment (with a 5-bit CCW CHAN field there are also four internal channels and an End-of-Queue control word). It should be understood by one of ordinary skill in the art that the channel field may optionally be increased or decreased to allow more or fewer channels.

The QADC module 1 has up to twenty external pins as shown in FIGS. 1 and 2. All of these pins except the power and reference pins can be used as general purpose digital port pins. Lower pin-count versions of the QADC module 1 can be produced by reducing the number of channel/port pins. Versions with as few as twelve pins may comprise eight analog channels, two power pins, and two reference pins.

CONTROL REGISTER AND LOGIC CIRCUIT

FIG. 3 shows a block diagram of Control Register and Logic circuit (shown generally within the dashed line and indicated by reference numeral 60) and various signal paths between it and Bus Interface Unit 70, CCW Table 62, Results Table 64, Address Decode circuit 66, and other circuitry shown in FIG. 2.

Control Register and Logic circuit 60 comprises Trigger Select & Priority circuit 200, Registers 210, Register Control & Decode circuit 220, Interrupt Logic 230, Queue Control & CCW Addressing circuitry 240, and ADC Sample Control & Conversion Control (indicated generally by reference numeral 250).

The Trigger Select & Priority circuit 200 is responsible for determining the type of trigger for initiating an A/D conversion sequence, in response to mode information from the Register circuitry 210. It is also responsible for selecting Queue 1 or Queue 2 for the conversion sequence in response to control information decoded by the control registers.

The Trigger Select & Priority circuit 200 is responsive to external trigger signals ETRIG1 and ETRIG2 via lines 203 and 204, respectively. Trigger Select & Priority circuit 200 is also coupled to the Periodic Timer 48 via line 205. Trigger Select & Priority circuit 200 is responsive to mode control signals from the control registers via line 213 and to an End-of-Queue (EOQ) signal from Queue Control & CCW Addressing circuitry 240 via line 242. Trigger Select & Priority circuit 200 generates control signals to Queue Control & CCW Addressing circuitry 240 via signal path 206.

It will be understood by those of ordinary skill in the art that the terms "signal path" or "line", as used herein, may refer to a single conductor or a multiple-conductor bus, or other suitable signal path, as appropriate to the implementation.

Register circuitry 210 comprises the registers shown in FIG. 6 and not otherwise shown in FIG. 2; i.e., a Module Configuration Register, a Test Register, an Interrupt Register, Control Registers 0-2, and a Status Register. The function of the Register circuitry 210 is to enable the automatic control of the operation of the QADC, once the registers are loaded by the host system software.

Register circuitry 210 generates control signals to the Sample Timer 46 via line 211, to the Prescaler 50 via line 212, to Trigger Select & Priority circuit 200 via line 213, to the Queue Control & CCW Addressing circuit 240 via line 214, and to Interrupt Logic 230 via line 221.

Register circuitry 210 receives control signals from Register Control & Decode circuit 220 via signal path 215 and an End-of-Queue (EOQ) signal from Queue Control & CCW Addressing circuit 240 via line 242.

Register circuitry 210 is also coupled to Bus Interface Unit 70 via bi-directional bus 217.

Register Control & Decode circuit 220 receives control and address information via busses 218 and 219, respectively, from Bus Interface Unit 70 and generates control signals to Register circuitry 210 via signal path 215. The function of Register Control & Decode circuit 220 is to provide control and addressing circuitry for the various registers within Register circuitry 210.

Interrupt Logic 230 operates to generate an interrupt signal to the host CPU upon conclusion of a conversion sequence (if enabled). Interrupt Logic 230 receives control signals from Register circuitry 210 via signal path 221 and an EOQ signal from Queue Control &

CCW Addressing circuit 240 via line 242. It is also coupled to the Bus Interface Unit 70 via signal path 231.

Queue Control & CCW Addressing circuitry 240 is responsible for controlling CCW addressing and the start of sampling and conversion operations. The Queue Control & CCW Addressing circuitry 240 receives control signals from the Trigger Select & Priority circuit 200 via line 206, from the Register circuitry 210 via line 214, and from the ADC Conversion Control circuit 254 via line 256. It generates control signals to the Trigger Select & Priority circuit 200, to the Register circuitry 210, and to the Interrupt Logic circuitry 230 via line 242. It also generates control signals to the Address Decode circuitry 66 via line 244, to the ADC Conversion Control circuit 254 via line 258, and to the ADC Sample Control 252 via line 251.

ADC Sample Control 252 is responsible for notifying the S/H circuits 40 and 42 (refer to FIG. 2), via the Sample Timer 46, to begin sampling. It is also responsible for notifying the ADC Conversion Control 254 when sampling is completed. The ADC Sample Control 252 receives control signals from Sample Timer 46 via line 262, from Queue Control & CCW Addressing circuit 240 via line 251, and from the CCW Table via line 253 (Input Sample Time) and line 255 (Re-sample Inhibit). It generates control signals to the Sample Timer 46 via line 261 and to the ADC Conversion Control 254.

The ADC Conversion Control 254 is responsible for initiating a conversion operation by the SAR 58 and for informing the Queue Control & CCW Addressing circuit 240 upon conclusion of the conversion operation. The ADC Conversion Control 254 receives control signals from the ADC Sample Control 252. It also receives control signals from the Queue Control & CCW Addressing circuit 240 via line 258, and it generates control signals to the SAR 58 via line 257.

As shown in FIG. 3, in response to a decoded CCW a REF control signal may be transmitted to the REF. MUX 26 via line 263, and a CHAN control signal may be transmitted to the CHAN. MUX 28 via line 264.

Upon conclusion of a conversion operation, a digital value is transmitted via line 265 from SAR 58 and stored in Results Table 65.

INTERMODULE BUS (IMB) INTERFACE

FIG. 4 is a table defining the Intermodule Bus (IMB) signals of the A/D converter module of the present invention.

The address bus IADDR and data bus IDATA, along with their associated control and handshake lines, are used to transfer data between the IMB 72 and the QADC module 1.

The reset signal IMSTRSTB initializes certain register bits to their default states. These default states are described in the register descriptions below. The master reset signal IMSTRSTB and system reset signal ISYSRSTB are used to reset the BIU (Bus Interface Unit) state machine.

ISIZ and IADDR are used to determine the size of data (byte or word). The QADC module 1 has certain bits that are only accessible in test mode, and the ITSTMODB line is used for test mode operation.

ADDRESS MAP

FIG. 5 shows an address map (indicated generally by reference numeral 75) for the control registers, Conversion Command Word table, and the Conversion Result Table of the A/D converter module.

The QADC module 1 utilizes 512 bytes, or 256 words, of address space, as shown in FIG. 5. Of the words actually implemented, 9 words are control, status, and port registers (indicated generally by reference numeral 80), 32 words are Conversion Command Words (indicated generally by reference numeral 81), and 32 words are used for each data format type of the result table (indicated generally by reference numerals 83, 85, and 89, respectively). The remaining words are reserved for possible future expansion.

The first block 80 of the address map 75 contains the 9 words used for control, status, and port information. These permit a host data processing system (not shown) to initialize the QADC module 1 into the desired configuration and mode of operation. Also included are status bits that the host system may read to identify an interrupt and to determine other information about the conversion operation of the QADC module 1. The content of these registers is shown in somewhat greater detail in FIG. 6.

The next block 81 of the address map 75 is the Conversion Command Word table. In the current embodiment there are up to 32 words to hold the desired A/D conversion sequences, but this could optionally be increased or decreased. A Conversion Command Word (CCW) is a 16-bit word, with eight implemented bits in four fields, and eight bits in optional control fields.

The content of the CCW 82 is illustrated in FIG. 7. Each CCW provides the converter with channel number (CHAN), input sample time (IST), reference pair (REF), and causes the converter to take an input sample, convert that analog value, and put the result in the corresponding word of the result register table. The CCW also includes a field RSI (re-sample inhibit). In addition the CCW may include one or more optional control fields if desired, such as a field to specify the converter resolution and a field to designate the data result alignment. The fields of the CCW and their functions are explained in greater detail below under the sub-heading "Conversion Command Word".

The result register can be read at the address ranges shown as Conversion Result Tables 83, 85, and 89. There is in actuality a single result register table but three different ways in which to read it, as explained in the section below entitled "A/D Result Data Format Options".

Thus there is one 32-word Conversion Result Table that appears in three places in the address map 75. The first block 83 presents the result data in right-justified (unsigned) format, the second block 85 is in left-justified (signed) format, and the third block 89 is a left-justified (unsigned) result.

Details on the control registers, status registers, port registers, and the CCW are provided below. Read accesses of reserved register locations or unused bits returns "0" and writes to reserved and unused space has no effect on the QADC operation.

CONVERSION COMMAND WORD TABLE

FIG. 8 is a conceptual diagram showing how Conversion Command Words are used to produce Result Words which are stored in the Conversion Result Table.

The central element in software control of the QADC module 1 is the Conversion Command Word Table. In a preferred embodiment, there are two queues

in the table which, depending on the application, can be operated in several different trigger modes and effective scan rates. It will be apparent to one of ordinary skill that more or fewer than two queues may be employed.

There are two reasons for including two queues in the QADC. One reason is that there are two different cases for automatically scanning analog input channels. One case is to get one sample from all or some analog input pins.

The other case is to automatically take multiple samples of one channel in rapid succession, so that host system software can use smoothing algorithms to calculate a more accurate value. In either case, an automatic scan that puts the results in a table saves the host system software from having to initiate each conversion, wait, get the result, and save it. The CCW table architecture permits the host system software to use either method, or even a combination; for example, 16 results could be used for four samples on each of four channels.

The other reason for providing two CCW queues is that two different operating modes can be used at the same time. Usually, analog inputs on some channels need to be converted often because they have rapidly changing values, whereas analog inputs on other channels change relatively slowly, such as temperature drift, battery voltage, and operator inputs.

In a preferred embodiment, Queue 1 is normally utilized for frequently occurring or time-critical conversion sequences. Queue 2 is normally utilized for relatively infrequent or non-time-critical conversion sequences. When a conversion sequence is initiated from Queue 1, any conversion in progress from Queue 2 is aborted. When the Queue 1 conversion sequence is completed, the aborted Queue 2 conversion sequence is restarted at its top location.

The host system software can receive an interrupt that occurs just after the Conversion Result Table has been filled with newly converted digital values from either queue. The interrupt permits the host system software to analyze newly converted values when they are fresh.

The host system software is relieved of the burden of initiating the A/D conversion sequence, of initiating each A/D conversion, and of moving each result to host system RAM. Thus the QADC module 1 absorbs the overhead of running the A/D converter system. The host system software only needs to program the QADC initially and then analyze the on-going results.

The following sections describe the basic operation of the CCW queues and the various modes that use the CCW queues.

CONVERSION QUEUE OPERATION

To prepare the QADC module 1 for a conversion sequence, the host system software fills up the table of Conversion Command Words (reference numeral 81 in FIG. 5 and reference numeral 62 in FIG. 8) to establish the desired conversion sequences. The host system software establishes the criteria for initiating the conversion sequences in Control Registers 1 and 2. Other registers also require initialization, for example, the Module Configuration Register, the Interrupt Register, and Control Register 0.

The sequences may be initiated (triggered) by a host system software command, the elapse of the QADC module periodic timer interval, an external trigger signal, or the completion of the previous conversion sequence (i.e. continuous mode). By whichever method the sequence of conversions is initiated., the conversions progress in the same way.

After the CCW table and all of the control registers are initialized, the QADC waits for a trigger condition for either queue. When triggered, the A/D converter obtains the first CCW from the triggered queue and executes it. Refer to FIG. 8.

The first part of a conversion is the sample phase. Once the sampled analog level is transferred to the converter, the sample-and-hold circuit proceeds with sampling the next channel.

The CCW specifies whether the sample time is to be the default time or an alternate time. For the first sample of a conversion sequence, the default sample time is a specified number of conversion clock cycles. For all subsequent samples the default sample time is the conversion time. The alternate sample time is chosen instead of the default when slower sample times are needed for high impedance sources or for specific delay intervals.

When each analog-to-digital conversion is complete, the result is written to the corresponding location in the Conversion Result Table. The converter then obtains the next CCW from the queue and proceeds with that conversion.

The QADC executes each CCW in the queue until one of three End of Queue (EOQ) indications is detected. One EOQ condition is reaching the physical end of the Queue RAM space, 32 locations in the preferred embodiment. The second EOQ condition is when the BQ2 pointer is reached (see FIG. 8), which indicates the split of the RAM between Queue 1 and Queue 2. This method applies only for indicating the end of Queue 1. The third indication is a CCW with an EOQ code instead of a normal channel selection. When enabled, Queue Conversion Sequence Complete Interrupts are issued to the host system software.

PRESCALER

The QADC module uses the IMB System Clock signal as the time base for conversions. The A/D conversion needs a clock signal in a fairly narrow range, and the IMB clock "Iclock" varies widely among applications. The Prescaler (50, FIG. 2) is a modulus-programmable divider that allows the A/D conversion clock to be within the specified range with a wide range of System Clock frequencies. The Prescaler can be used to optimize the A/D conversion time by selecting a System Clock frequency that is an even multiple of the fastest A/D conversion time.

PERIODIC TIMER

It is known in prior A/D conversion systems to use a periodic processor interrupt to begin a conversion sequence of an analog channel or group of analog channels. While the conversion is in progress, the processor attempts to accomplish other work or waits for the A/D conversion to complete. In many real-time applications, this software burden unacceptably impacts the performance of the system. Ideally, a processor need become involved only when converted results are available from the A/D converter module.

Thus, the QADC includes a dedicated periodic interval timer (48, FIG. 2), which, when enabled, automatically initiates A/D conversion sequences. Queue 2 can be programmed to operate in the periodic interval mode. The host system software selects the periodic mode and determines the time interval via Control Reg-

ister 2. Typically, the host system software would also enable the corresponding Completion Interrupt. This interrupt notifies the host system software that new analog conversion results are available.

In operation, when the timer interval elapses, the queue execution is initiated. Once started, conversion can automatically occur repetitively over multiple channels, if enabled, thus relieving the host system software of the burden of getting the results of each conversion and initiating the next conversion.

Often one queue is configured in the periodic mode and the other queue is set up for one of the other operating modes. For low priority scans, the periodic mode uses somewhat less power than the continuous mode.

Periodic analog conversion allows the host system software to be in synchronization with the hardware conversion scan by including notification that the conversions have just finished. This provides the software the time until the next period in which to read the results, and to know that the values were all read in one sequence, whereas a continuous scan mode does not allow the software to easily conclude that samples of two channels were contiguous data, taken during the same scan.

EXTERNAL TRIGGER

There are applications that need to synchronize the sampling of analog channels to external events occurring elsewhere in the system. These external events can relate to external timers or system events, for instance, or sense physical conditions, such as an index position of a moving device.

In prior art micro-controllers, software must determine the correct time to start a conversion and then start it at the right time, but due to system latencies (e.g. interrupts, long instructions), it may be difficult to predict the starting time accurately. It is also known, regarding prior art micro-controllers, for the software to use an external interrupt to synchronize the conversions. However, with variable interrupt response time, conversions begin imprecisely in relation to the external signal or event. In many applications, the sample must be taken at a precise time.

An external hardware signal permits a direct path that is independent of software timing errors to start the conversion. The present invention does not rely on software initiation of the conversion start but allows a signal or event which is external to a micro-controller, of which the QADC may be a part, to start the conversion. The external trigger, when implemented with an automated queue or conversion sequence, as in the present invention, allows the A/D converter to collect analog data independent of a host CPU located on the micro-controller or elsewhere.

It is known in stand-alone A/D converters to employ an external trigger to initiate a single conversion. However, the present invention permits an external trigger signal or event to repetitively initiate conversion sequences.

The next external conversion may be enabled when the A/D converter has completed its current set of conversions and an external trigger is asserted. Alternatively, the conversion may restart immediately on assertion of the external trigger signal during a conversion sequence, if the implementation of the external start function is so defined.

The QADC module allows External Trigger input pins to initiate a conversion sequence on Queue 1 and Queue 2.

One usage is to take analog samples at a precise point in the motion of a high speed device, such as an engine. The ability to initiate a conversion in response to an external trigger is very useful in the automotive control environment, since conversions can be synchronized to engine position. There is not time for host system software initiation of the A/D conversions since host system software interrupt response time varies. The source of the External Trigger signal may be the output of a timer channel. The polarity of the trigger signal is programmable, so that the host system software can choose the rising or falling edge to initiate the sequence.

The use of the queue is the same in the External Trigger mode as with the other modes. The trigger signal simply initiates the sequence, rather than the interval timer, as in the periodic mode. Each CCW is obtained and the indicated conversions are performed until one of the End of Queue indications is encountered. When the sequence is complete, the Completion Interrupt is issued, if enabled, and the queue waits for the next edge on the External Trigger pin.

CONTINUOUS CONVERSIONS

In the preferred embodiment, only Queue 2 can be configured to operate continuously, since a continuous scan on Queue 1 would preclude the operation of Queue 2. When the last address or last-command indication is encountered in Queue 2, the sequence starts over with the top CCW in Queue 2. The continuous mode keeps the Conversion Result Tables updated automatically. The host system software can always read the Conversion Result Table and be assured that the value is no older than the scan time for both queues. The Completion Interrupt may be enabled to notify the host system software of the completion of each cycle through the queue.

SOFTWARE INITIATED CONVERSION

The above modes have shown three ways to automatically initiate conversions: periodically, upon external trigger stimulus, and continuously. To cover other situations, the host system software can also initiate a conversion sequence. A specific bit pattern in the mode word MQ1 or MQ2 of Control Register 1 or 2, respectively, starts each respective queue at its top CCW. The QADC automatically performs the conversions in the queue until an End of Queue condition is found. Then it stops and resets the mode field (MQ1 or MQ2) to the disabled condition. The next conversion sequence is triggered by a new host system software control word. This mode provides a one-shot scan through the CCW queue.

EXTERNAL MULTIPLEXED INPUTS

The number of analog inputs to the QADC may be expanded in the externally multiplexed mode. The full flexibility of the automatic scanning queues are available to externally multiplexed channels. Three of the analog channels (MA0-MA2, FIG. 1) are redefined to act as address bit outputs, and three input pins (ANx, ANy, and ANz) are expanded to represent eight input channels each. This allows a total of three external multiplexers for a total of 24 external channels. Commercially available analog multiplexers such as the MC14051, MC14052, MC74HC4051, and

MC74HC4052 available from Motorola, Inc. may be used.

FIG. 1 provides an example of externally expanding the number of channels in this manner. The preferred embodiment may be used with 0, 1, 2, or 3 external MUX's.

FIG. 9 is a table illustrating how the 5-bit CHAN field in the CCW specifies the functions of the various I/O pins for 0, 1, 2, or 3 external multiplexer IC's.

For example, with MUX field in Control Register 0 equal to 00 (i.e. no external MUX), CHAN field = 10000 designates Analog Input pin AN16.

Referring now also to FIG. 1, with MUX field equal to 01 (i.e. one external MUX), one of the inputs into MUX 10 (AN16, AN18, AN20, AN22, AN24, AN26, AN28, or AN30) is selected and coupled into pin ANx by the appropriate CHAN field value 1XXX0. For example, CHAN field 10000 selects input AN16; CHAN field 10010 selects input AN18; and so on.

With MUX field equal to 10 (i.e. two external MUX's), the appropriate input to MUX 10 is selected and coupled into pin ANx by the appropriate CHAN field value 1XXX0, as mentioned immediately above, and, in addition, one of the inputs into MUX 12 (AN17, AN19, AN21, AN23, AN25, AN27, AN29, or AN31) is selected and coupled into pin ANy by the appropriate CHAN field value 1XXX1. For example, CHAN field 10001 selects input AN17; CHAN field 10011 selects input AN19; and so on.

With MUX field equal to 11 (i.e. three external MUX's), the appropriate inputs to MUX's 10 and 12 are selected and coupled into pins ANx and ANy, respectively, as mentioned immediately above, and, in addition, one of the inputs into MUX 14 (AN8, AN9, AN10, AN11, AN12, AN13, AN14, or AN15) is selected and coupled into pin ANz by the appropriate CHAN field value 01XXX. For example, CHAN field 01000 selects input AN8; CHAN field 01001 selects input AN9; and so on.

For all external multiplexer modes, three of the internally multiplexed pins (AN18, AN20, and AN22) become multiplexer address outputs MA0, MA1, and MA2, respectively.

FIG. 9 shows that either three, two, one, or no external multiplexers can be used, and that the use of the I/O pins varies. The channel numbers used by the host system software in the CCW's varies too with the different multiplexing modes. It will be apparent to one of ordinary skill in the art that the herein-disclosed method of sampling external MUX's may be utilized with MUX's with fewer or more analog input pins, and that the number of MUX's may be varied.

FIG. 10 is a table which shows the number of analog channels available with different numbers of external multiplexer chips for the various implementations possible, in terms of the number of I/O pins allocated to the QADC module 1. For example, in the 18-pin version, a total of fourteen analog channels are available with no external MUX chips; eighteen analog channels are available with one external MUX chip; twenty-five analog channels are available with two external MUX chips; etc.

SIMULTANEOUS SAMPLING

Simultaneous sampling may be used for receiving and converting differential or other special signal pairs. The QADC allows two adjacent analog input channels, identified by ignoring the lowest-order bit of the CHAN field in the CCW, to be sampled at the same time. Two adjacent analog channels are always sampled simultaneously, but only one is converted with each CCW. To convert a simultaneous analog sample from the second channel, the CCW inhibits re-sampling in the next CCW.

INPUT SAMPLE TIME

The sample time may be altered through host system software control. Different analog signal source impedances may thus be used. Allowing higher source impedances can eliminate the cost of an external amplifier. The trade-off is a longer sample time.

By host system software selection, the system clock and prescaler output (based on the system clock) are used as a time base (an on-chip RC oscillator might also be used as a time base). One input sample time is the default minimum, and the other sample time is programmed by the host system software. The default sample time is a specified number of clock cycles for the first conversion of a sequence and is the A/D conversion time for subsequent channels in a conversion queue. When the default sample time is too fast, the host system software can specify a longer sample time, and that sample time is programmable for up to 128 QADC clock cycles in a preferred embodiment.

ALTERNATE REFERENCE INPUTS

There are two sets of reference pins for A/D conversion. Each analog channel may be referenced to either the primary or alternate pair of reference voltages. The primary reference pins are V_{RH0} and V_{RL0}, and the alternate reference pins are V_{RH1} and V_{RL1}. The alternate reference pins also may be input channels when not needed as references, or they can be converted to compare or calibrate the reference levels. Note that the reference pins may be separated from the supply pins in some implementations or shared with them in other implementations.

A/D RESULT DATA FORMAT OPTIONS

FIG. 11 illustrates the data format options of Result Words stored in the Conversion Result Table. The QADC 1 includes a table of Conversion Result Registers, readable in any of at least three data format options for each Result Word.

One option is with the 10-bit result right-justified in the 16-bit word, with zeros in the higher order unused bits. Another choice is a left-justified result with zeros in the lower order unused bits. The third option is a left-justified result with the most significant bit inverted and with zeros in the unused lower order bits. This third option corresponds to a "half-scale, offset binary, twos-complement" data format, which is useful in digital signal processing applications. Another option, not implemented in the embodiment illustrated herein, is a right-justified, signed format. In addition, a right-justified, sign-extended format (with leading 0's or 1's, depending upon the sign) could be provided.

The Conversion Result Registers are 10 bits wide. In the present embodiment the remaining six bits of each 16-bit word are not implemented. The result data formatting is produced during host system software read operations, since the address range where the results are read is used to select the desired data format. Refer to FIGS. 21 and 22, and the accompanying description below under the heading "Result Word Format Op-

tions", for further information concerning the various data format options.

Write operations, including read-modify-write instructions like bit manipulation, do not access a true 16-bit value. Since the 10-bit result is stored in a 10-bit register or memory word, 6 bits are saved, thereby reducing the silicon area of the integrated circuit.

REGISTER DESCRIPTIONS

This section discusses the detailed formats of the control, status, digital port, and CCW information that the host system software provides to the QADC and obtains from the QADC. Four types of word format are discussed in the following subsections. First are the control words that the host system software provides to configure and initialize the QADC module. Second are the digital data ports. Third is a status word that the host system software reads to determine the current operation of the QADC, including interrupt flags. Last is the Conversion Command Word for each A/D conversion that is obtained from the CCW queue.

MODULE CONFIGURATION REGISTER (MCR)

FIG. **12** shows the format of the Module Configuration Register of the A/D converter module.

The Module Configuration Register includes initialization information from the host system software to the QADC. This information is typically set up once on power-up and not changed during normal operation, though it may be changed when needed. Included are stand-by mode selection, supervisor space selection, and interrupt arbitration.

STOP-Stop Mode (Bit Position: **15**)
Function: Stop mode select (stop clocks, power down analog circuits)
Reset State: STOP=0

The host system software can disconnect the clock signal to the A/D converter and power down the analog circuits to reduce power. When set, the STOP bit aborts any conversion sequence in progress. Because the bias currents to the analog circuits are turned off, the QADC module requires some recovery time to stabilize the analog circuits after clearing the STOP bit.

FRZ-Freeze Enable (Bit Position: **14**)
Function: Freeze Enable (suspend module operation)
Reset State: FRZ=0

When debugging an application, it is useful in many cases to have the QADC module pause when a breakpoint is encountered. When FRZ=1 and the IMB's IFREEZEB signal is asserted, the current conversion is aborted, and the queue is left in a mode noting that it needs service. The QADC clock is stopped so that the periodic timer is not advancing either. Any external trigger events that occur during the freeze mode are not recorded. When the IMB's IFREEZEB signal is negated, conversions begin again at the top of the queue. If neither queue is awaiting service when the freeze mode is exited, the module waits for an appropriate queue trigger to occur.

SUPV Supervisor Space (Bit Position: **7**)
Function: Supervisor space selection
Reset State: SUPV=1

Some host CPU's and software systems permit two addressable spaces: unrestricted space accessible to any software, and supervisor space which is accessible only from system software (the operating system). Other host CPU's do not include this option and are thus always in the supervisor mode from the vantage point of the QADC. The first three register word locations in the RAM register table (**80**, FIGS. **4** and **5**), which are the Module Configuration Register, Test Register, and Interrupt Register, are always in the supervisor space. The remaining Control, Status, and Port registers are programmable via the SUPV bit.

FIG. **13** illustrates the use of the SUPV bit of the Module Configuration Register of the QADC. When SUPV=1, all QADC Status, Control, and Port registers are accessible only in the Supervisor mode. When SUPV=0, they may be accessed in either the Supervisor or unrestricted modes. When the QADC is used with a host CPU that does not support Supervisor/unrestricted modes, the state of the SUPV bit is unimportant.

IARB Interrupt Arbitration Number (Bit Position: 0-3)
Function: Define interrupt arbitration priority number
Reset State: IARB=0001

Within the QADC, the interrupt level is assigned to each interrupt source via the Interrupt Register (FIG. **14**). Since multiple IMB modules could request an interrupt on each interrupt level, the priority of the interrupt within the assigned level is established with the IARB field.

Once the host CPU begins to process an interrupt request at a particular level, an arbitration cycle determines which interrupt is to be served of those requesting on that level. The **0000** state of IARB is not valid, leaving up to 15 IMB modules that can arbitrate for interrupt service. The lowest priority is 0001 and the highest is 1111.

It is the responsibility of the initialization host system software to ensure that the seven bits that establish the interrupt level and priority (INL1 and INL2, plus IARB) are unique throughout the entire system. Successful interrupt arbitration depends on no two interrupts causing the same level and priority to be used on the Intermodule Bus (IMB).

TEST REGISTER

The Test Register controls various test modes which are used during manufacturing, and is not intended to be used in a normal application. The Test Register can only be written in the test mode, when the ITSTMODB line on the IMB is asserted. In the non-test mode the Test Register can only be read, but writes have no effect.

INTERRUPT REGISTER

The Intermodule Bus (IMB) requires three things to fully identify an interrupt request. First, the request must be asserted on one of seven levels. Since the QADC module has two separate interrupt request sources, two 3-bit software-provided parameters establish the request level for each source. Then, one of 15 possible priorities within that level is determined by an arbitration process on the IMB. The QADC includes 4-bits in the Module Configuration Register for the arbitration priority. Third, an 8-bit vector number is provided on the IMB to identify the software entry point for each interrupt source.

FIG. **14** shows the format of the Interrupt Register of the A/D converter module.

INL1-Interrupt Level 1 (Bit Position: **12-14**)
Function: Define Queue **1** interrupt level
Reset State: INL1=000

Three bits are used for the host system software to assign the Queue **1** Completion Interrupt to one of

seven interrupt levels. The 000 state disables the interrupt. Level 001 is the lowest priority interrupt level, and level 111 is the highest. The QADC uses the level number to determine which of seven interrupt requests to the host CPU is to be asserted. The host CPU permits the interrupt to occur when there are no other interrupts at a higher level. Up to 15 different interrupts can be assigned by the host system software to a particular interrupt level, provided that each is assigned a unique interrupt priority.

INL2-Interrupt Level 2 (Bit Position: 8–10)

Function: Define Queue 2 interrupt level

Reset State: INL2=000

Three bits are used for the host system software to assign the Queue 2 Completion Interrupt to one of seven interrupt levels. The 000 state disables the interrupt. Level 001 is the lowest priority interrupt level, and level 111 is the highest. The QADC uses the level number to determine which of seven interrupt requests to the host CPU is to be asserted. The host CPU permits the interrupt to occur when there are no other interrupts at a higher level. Up to 15 different interrupts can be assigned by the host system software to a particular interrupt level, provided that each is assigned a unique interrupt priority.

INTV-Interrupt Vector Number (Bit Position: 0–7)

Function: Define interrupt vector

Reset State: $0F

The Interrupt Vector Number is established by the host system software. The QADC uses two interrupt vectors, one for each of the CCW queues. Therefore, the host system software writes the high order seven bits of the Interrupt Vector Number into the QADC Interrupt Register. The QADC provides the eighth bit back to the host CPU during a bus IACK (interrupt acknowledge) cycle.

An interrupt from CCW Queue 1 completion returns an interrupt vector of binary xxxx xxx0, where xxxx xxx is the INTV field. An interrupt from a CCW Queue 2 completion causes the returned vector to be xxxx xxx1. The vector number identifies the place in memory where the host CPU obtains the program counter for the interrupt routine. The Interrupt Vector Number is independent of the interrupt level and arbitration priority.

PORT DATA REGISTER

All QADC pins that are not needed for their analog inputs, external trigger inputs, or external multiplexer interfacing, can also be used as digital port pins. The following descriptions refer to the highest pin-count version of the module, operating in the internally multiplexed mode. With the versions that implement fewer pins, the full width of the digital ports is not available.

FIG. 15 shows the formats of the 8-bit Port A and Port B Data Registers of the A/D converter module.

Port A Data Registers (Bit Position: 8–15)

Function: Input/output data register

Port A is a bi-directional 8-bit I/O port that may be used for general purpose digital input or output signals.

Port B Data Register (Bit Position: 0–7)

Function: Input data register

Port B is an input-only 8-bit digital port that may be used for general purpose digital input signals.

PORT DATA DIRECTION REGISTER

The Data Direction Register (DDR) associated with a digital I/O port establishes whether each bi-directional pin is an input or an output.

FIG. 16 shows the format of the Port A Data Direction Register of the A/D converter module.

Port A Data Direction Register (Bit Position: 8–15)

Function: Establish Port A pin functions as input or output

Reset State: $00

In the maximum pin-count configuration, all eight bits of Port A are bi-directional. The Data Direction Register bits associated with each pin establish whether the pin handles an input or an output signal. On power-up, the Data Direction Register is reset, and all port pins are inputs. The host system software selects a pin to be a driven output signal by writing a binary one into the Data Direction bit for the pin. When the DDR establishes a pin to be an output, a host system software read of the Port A Data Register obtains the state of the output port data register, not the actual pin, in order to permit read-modify-write instructions.

CONTROL REGISTER 0

FIG. 17 shows the format of Control Register 0 of the A/D converter module.

Control Register 0 includes initialization information for the entire converter, not just one of the CCW queues. Some of the control fields in this word establish parameters that are referenced by the CCW.

MUX External Multiplexed Modes (Bit Position: 14,15)

Function: Enable externally multiplexed channel selection

Reset State: 00

The host system software can enable an expansion of the number of channels by setting the MUX mode. When MUX=00, a maximum of 16 channels are available. MUX=01, enables expansion with one external multiplexer chip.

In each of the external multiplexed modes, the PA0, PA1, and PA2 pins become multiplexed address output pins (MA0, MA1 and MA2), thereby out-putting three bits from the 5-bit CHAN field of the CCW. The PB1 pin becomes the multiplexed channel analog input pin, ANx.

MUX=10 enables the expansion for two external multiplexers. In this mode, PB2 becomes the additional multiplexed analog input pin, ANy. The ANx pin is used for all even channels in the range of 16–30. Similarly, the ANy pin, serves all odd channels in the range of 17–31. These two inputs may serve as a pair, thus extending the simultaneous sample function to the externally multiplexed channels.

MUX=11 enables the expansion for three external multiplexers. In this mode, the PB3 pin becomes the additional multiplexed channel analog input pin, ANz. The main use for this mode is when only 10 to 14 pins can be allocated to the QADC module on the overall integrated circuit of which it is a part.

The following table summarizes the four states of the MUX field:

MUX=00 Internally multiplexed, 16 possible channels

MUX=01 Externally multiplexed (1 Unit), 20 possible channels

MUX=10 Externally multiplexed (2 Units), 27 possible channels

MUX=11 Externally multiplexed (3 Units), 27 possible channels, plus digital port pins

IST1 Input Sample Time (Bit Position: 8,9)

Function: Select input sample time for CCW IST bit=1

Reset State: 00

For channels connected to higher source impedances, a longer sample time is required to ensure conversion accuracy. Other signals need to be converted as quickly as possible. The IST bit in the CCW selects which of two sample times are to apply to that conversion. When the CCW IST=1, the two IST1 bits in Control Register 0 establish the input sample time. There are four selectable input sample times in the present embodiment:

IST1 = 00	Input Sample Time = Tadcck × 16
IST1 = 01	Input Sample Time = Tadcck × 32
IST1 = 10	Input Sample Time = Tadcck × 64
IST1 = 11	Input Sample Time = Tadcck × 128

PRES Prescaler (Bit Position: 0–4)

Function: Define IMB System Clock to QADC Operating Clock ratio.

Reset State: 1111

The QADC Operating Clock Time (Tadcck) is the time-base for all A/D conversion functions, including the input sample time, the conversion time, and the periodic timer. The pre-scaling is between the IMB System Clock (Iclock signal) and the Tadcck internal clock of the QADC module. The prescaler must be host system software programmed so that its output frequency falls within the Tadcck tolerance.

In order to permit wide selection of the System Clock (Tclock) frequency, the QADC prescaler is modulus-programmable. A 4-bit modulus prescaler, followed by a divide-by-two stage to ensure clock symmetry, multiplies the System Clock period by from 2 to 30, in even integer increments, as shown in the following table:

	Operating Clock Time
PRES = 0000	QADC Clock Time (Tadcck) = Tclock × 2
PRES = 0001	QADC Clock Time (Tadcck) = Tclock × 4
PRES = 0010	QADC Clock Time (Tadcck) = Tclock × 6
PRES = 0011	QADC Clock Time (Tadcck) = Tclock × 8
PRES = 0100	QADC Clock Time (Tadcck) = Tclock × 10
to	
PRES = 1101	QADC Clock Time (Tadcck) = Tclock × 28
PRES = 1110	QADC Clock Time (Tadcck) = Tclock × 30
PRES = 1111	QADC Clock Time (Tadcck) = Tclock × 32

CONTROL REGISTER 1

FIG. 18 shows the format of Control Register 1 of the A/D converter module.

Control Register 1 is the Mode Control Register for the operation of Queue 1. The host system software establishes the operating mode of the queue servicing logic. One key purpose is to establish the criteria for beginning a conversion sequence with the first CCW in the queue. The first conversion can be initiated by an external signal, or by host system software command. Control Register 1 also allows the host system software to enable a Conversion Complete Interrupt.

CIE1-Completion Interrupt Enable 1 (Bit Position: 15)

Function: Enable interrupt upon completion of Queue 1

Reset State: 0

CIE1=0 disables the Conversion Complete Interrupt associated with Queue 1. CIE1=1 enables an interrupt after the last conversion of a Queue 1 CCW sequence. The last conversion in the sequence is identified when the CCW pointer is at the beginning of Queue 2, an end-of-queue code is encountered in the CHAN field of the CCW, or the end of the queue RAM is reached.

MQ1-Mode, Queue 1 (Bit Position: 8,9)

Function: Select the operating mode for Queue 1

Reset State: 00 (binary)

Two bits establish the operating mode of Queue 1 in the CCW Table. These bits are written to Control Register 1 by the host system software. The only case when they are modified by the QADC is the Software Initiated mode, where the mode is changed to the disabled state after one conversion sequence. When there are active CCW's in Queue 1 awaiting service by the analog subsystem (sample and hold, and A/D converter), they have priority over any pending CCW's in Queue 2. The mode selected for MQ1 and the channels assigned to Queue 1 are thus the high priority A/D conversions. Therefore, Queue 1 does not include a continuous mode, since this would preclude the operation of Queue 2.

The following summarizes the operating modes of Queue 1:

MQ1=00 Disabled, no conversions

MQ1=01 Software initiated, starts conversion sequence with the act of loading 01 into MQ1

MQ1=10 External trigger 1, positive edge starts conversion sequence

MQ1=11 External trigger 1, negative edge starts conversion sequence

CONTROL REGISTER 2

FIG. 19 shows the format of Control Register 2 of the A/D converter module.

Control Register 2 is the Mode Control Register for the operation of the CCW's in Queue 2. The host system software establishes the operating mode of the queue servicing logic, that is, the criteria for beginning a conversion sequence with the first CCW in Queue 2. The first conversion can be initiated by host system software command, at regularly timed intervals, immediately after the last sequence is completed (the continuous mode), or when an external trigger occurs.

CIE2-Completion Interrupt Enable 2 (Bit Position: 15)

Function: Enable interrupt upon completion of Queue 2

Reset State: 0

CIE2=0 disables the Conversion Complete Interrupt associated with Queue 2. CIE2=1 enables an interrupt after the last conversion of a Queue 2 CCW sequence. The last conversion in the sequence is identified when the CCW index pointer is at the last location of the table or the CCW CHAN field is the end-of-queue code.

MQ2 Mode, Queue 2 (Bit Position: 12–14)

Function: Select the operating mode for Queue 2

Reset State: 0000 (binary)

Four bits establish the operating mode of Queue 2 in the CCW Table. These bits are written to Control Register 2 by the host system software. The only case when they are modified by the QADC is the Software Initiated mode, where the mode is changed to the disabled state after one conversion sequence. When there are active CCW's in Queue 1 awaiting service by the analog subsystem (sample and hold, and A/D converter), they have priority over any pending CCW's in Queue 2. The mode selected and the channels assigned to Queue 2 should thus be the lower priority A/D conversions.

With prior art A/D converters integrated into microcontroller units, a common software usage is for a

periodic interrupt (real-time clock interrupt) routine to initiate an A/D conversion sequence. The QADC includes a periodic timer to keep the host system software from having to initiate a conversion scan. The MQ2 field selects the periodic mode and establishes the time interval.

Periodic Timer Interval	
MQ2 = 0000	Disabled, no conversion
MQ2 = 0001	Software initiated, start conversion sequence with the act of loading 0001 into MQ2
MQ2 = 0010	External trigger 2, positive edge starts conversion sequence
MQ2 = 0011	External trigger 2, negative edge starts conversion sequence
MQ2 = 0100	Continuous mode
MQ2 = 0101	Periodic timer interval = Tadcck × 128
MQ2 = 0110	Periodic timer interval = Tadcck × 256
MQ2 = 0111	Periodic timer interval = Tadcck × 512
MQ2 = 1000	Periodic timer interval = Tadcck × 1024
MQ2 = 1001	Periodic timer interval = Tadcck × 2048
MQ2 = 1010	Periodic timer interval = Tadcck × 4096
MQ2 = 1011	Periodic timer interval = Tadcck × 8192
MQ2 = 1100	Periodic timer interval = Tadcck × 16384
MQ2 = 1101	Periodic timer interval = Tadcck × 32768
MQ2 = 1110	Periodic timer interval = Tadcck × 65536
MQ2 = 1111	Periodic timer interval = Tadcck × 131072

BQ2 Beginning of Queue 2 (Bit Position: 0–4)

Function: Indicates the CCW address where Queue 2 begins

Reset State: 11111

To allow the length of Queue 1 and Queue 2 to vary, a pointer initialized by the host system software is used to identify the CCW table location where Queue 2 begins. BQ2 is used to detect the end of Queue 1, as well as the initial position for Queue 2. If Queue 2 is interrupted by the higher priority Queue 1, Queue 2 automatically restarts at its top location after Queue 1 is completed.

STATUS REGISTER

The Status Register may be read by the host system software and contains information associated with the conversion queues and the overall QADC module.

FIG. 20 shows the format of the Status Register of the A/D converter module.

CCF1-Conversion Complete Flag 1 (Bit Position: 15)

Function: Indicates Queue 1 conversion sequence completion

Reset State: 0

The Conversion Complete Flag 1 is set by the QADC when the last conversion of Queue 1 is finished. CCF1 is a status bit that is available to the host system software whether or not the corresponding interrupt is enabled. When CCF1=1, the interrupt is enabled (CIE=1), and the interrupt level field (INL1) is a non-zero value, the QADC creates an interrupt request to the host CPU using the level (INL1) in the Interrupt Register, the priority (IARB) in the Module Configuration Register, and the vector number (INTV) in the Interrupt Register. The CCF1 flag is cleared back to zero when it is written to zero and it was a one when last read.

CCF2-Conversion Complete Interrupt Flag 2 (Bit Position: 14)

Function: Indicates Queue 2 conversion sequence completion

Reset State: 0

The Conversion Complete Flag 2 is set by the QADC when the last conversion of Queue 2 is finished. CCF2 is a status bit that is available to the host system software whether or not the corresponding interrupt is enabled. When CCF2=1, the interrupt is enabled (CIE2=1), and the interrupt level field (INL2) is a non-zero value, the QADC creates an interrupt request to the host CPU using the level (INL2) in the Interrupt Register, the priority (IARB) in the Module Configuration Register, and the vector number (INTV) in the Interrupt Register. The CCF2 flag is cleared back to zero when it is written to zero and it was a one when last read.

BSY-Busy (Bit Position: 13)

Function: Indicates a sample/hold or conversion in progress.

Reset State: 0

When a CCW from Queue 1 or Queue 2 is in the process of being served by the sample and hold and/or the A/D converter, the BSY status bit is set to a one. When the analog subsystem is not actively serving either queue, the status bit is a zero.

CWP-Command Word Pointer (Bit Position: 0–4)

Function: Indicates the address of the current or last CCW to execute

Reset State: 00000 (binary)

The Conversion Command Word (CCW) table length is 32 words long. A 5-bit status field is included to allow the host system software to see which CCW is executing at present or was last completed. The host system software can thus monitor progress of a conversion sequence. When the converter is busy, the CWP shows the CCW being served. When not busy, CWP indicates the last CCW that was completed.

CONVERSION COMMAND WORD

The entries in the Conversion Command Word (CCW) table are 8-bit CCW's. The CCW is written by the host system software and is not modified by the QADC. The CCW contains the command bits to take one analog level sample and convert it to a digital result. The low-order bits of the CCW (CHAN, IST and RSI) contain command information for the sample and hold portion of the A/D converter. The REF bit of the CCW specifies the reference pair to use during conversion. The fields of the CCW will now be explained.

REF-Alternate Reference Enable (Bit Position: 7)

Function: Select primary or alternate reference for conversion process

Reset State: Not initialized

When the REF bit is a zero, the V_{RH0} pin is used for the high reference level, and V_{RL0} pin is used for the low reference level for the conversion. When the REF bit is set to one, the alternate high and low reference voltages, V_{RH1} and V_{RL1}, are used instead.

RSI-Re-Sample Inhibit (Bit Position: 6)

Function: Inhibits re-sample of analog input for simultaneous sampling

Reset State: Not initialized

In normal operation (RSI=0), two adjacent channels are sampled simultaneously, but only the one indicated by the CCW CHAN field is converted. When the user wishes to convert the simultaneously sampled adjacent channel, the RSI bit of the CCW is set to a one, to inhibit re-sampling. The lowest order bit of the CHAN field acts as a toggle between the two channels selected by the higher order bits in the CHAN field. Channel 1

cannot be simultaneously sampled since it is paired with channel 0, which is the code for the last CCW.

IST-Input Sample Time (Bit Position: 5)

Function: Selects one of two input sample times

Reset State: Not initialized

When the IST bit in the CCW is a 0, one of two default input sample times is used. For the first conversion of a sequence (the first CCW in Queue 1 and Queue 2), the default sample time is a few cycles, and for subsequent conversions in the queue, the sample time is the conversion time. When the IST bit in the CCW is a 1, the IST1 field in Control Register 0 is used to select the input sample time.

CHAN-Channel Number (Bit Positions 0-4)

(Function: Select input channel number)

Reset State: Not initialized

The CHAN bits select which analog input signal is connected to the A/D converter. When the MUX bits in Control Register 0 are clear, the QADC module is in the internally multiplexed mode. In this mode, the five CHAN bits enable the QADC to select up to 16 input channels, depending on the module version, plus internal test channels, as shown in FIG. 9. For micro-controller implementations with fewer than 16 external channels, the unconnected pins are connected to V_{DDA}/V_{RH0} or V_{SSA}/V_{RL0}.

When the MUX bits in Control Register 0 are not 00, one of the externally multiplexed modes is in use. The five CHAN bits are re-mapped, so that some of the channel numbers are externally multiplexed. The table in FIG. 9 shows the definition for the CHAN channel numbers for each multiplexing mode.

One of the CHAN words (CHAN=00000) is used as an end-of-queue indication instead of a multiplexed input channel. When the control logic encounters this end-of-queue code in the CCW table, no further conversions are performed on that scan through the queue.

In addition, as mentioned above, the CCW may include one or more optional control fields if desired. For example, a field may specify the converter resolution if different converter resolutions need to be accommodated. Another field may be used to designate the data result alignment, rather than using the two upper address bits to select the data result alignment in the manner explained immediately below.

While it is a significant advantage of the present invention that sampling and conversion operations can be conducted, once the queues are loaded by the host system software, without further involvement by such software, it is also possible for the host system software to dynamically modify information stored in the queues. This would normally be done only to the lower priority queue (e.g. Queue 2), since the higher priority queue (Queue 1) is normally utilized for high duty cycle operations on relatively fast changing signals.

One purpose in modifying the Queue 2 control information is to designate the periodic sampling and conversion of analog signals which typically change relatively slowly compared to those being sampled and converted under the control of Queue 1.

RESULT WORD FORMAT OPTIONS

FIG. 21 illustrates the addresses (i.e., absolute addresses, where "x" represents an arbitrary base address of the QADC module) required to read Result Words stored in the Conversion Result Table in at least three different data format options. The addresses are $XA0, $XA2, $XA4, etc., through $XDE for the thirty-two result words RSLT0 through RSLT31, respectively, in the right-justified, unsigned format.

The addresses are $X120, $X122, etc., through $X15E for the thirty-two result words RSLT0 through RSLT31, respectively, in the left-justified, signed format.

And the addresses are $X1A0, $X1A2, etc., through $X1DE for the thirty-two result words RSLT0 through RSLT31, respectively, in the left-justified, unsigned format.

FIG. 22 shows a detailed logic implementation of the Data Format logic 68 shown in FIG. 2. The 10-bit result word is read from the Results Table 64 via 10-bit bus 65, and each bit (RESULT [0] through RESULT [9]) is received by a respective line 140-149.

Two upper address bits are received by the Sign Control 130 and Left/Right Justify Control 132 lines. Lines 130 and 132 are input into NAND gate 134, whose output forms one input into Exclusive OR gate 180.

Left/Right Justify Control line 132 is also coupled via line portion 137 to the non-inverting control terminals of a first series of transmission gates 150-165 and to the inverting control terminals of a second series of transmission gates 150'-165'.

Left/Right Justify Control line 132 is also coupled via line portion 138 to inverter 136, whose output is coupled to the inverting control terminals of the first series of transmission gates 150-165 and to the non-inverting control terminals of the second series of transmission gates 150'-165'.

The input terminals of transmission gates 150'-159' are coupled to RESULT[0]-RESULT[9] lines 140-149, respectively, and their output terminals are coupled to inverters 150"-159", respectively. The input terminals of transmission gates 160'-165' are tied to ground.

The input terminals of transmission gates 156-165 are also coupled to RESULT[0]-RESULT[9] lines 140-149, respectively, and their output terminals are coupled to inverters 156"-165", respectively. The input terminals of transmission gates 150-155 are tied to ground.

The outputs of inverters 150"-164" represent DATA[0] through DATA[14], respectively.

The outputs of transmission gates 165 and 165' are coupled to the second input to Exclusive OR gate 180, whose output is DATA[15].

Outputs DATA[0] through DATA[15] are coupled to a 16-bit bus 67 which in turn is coupled to the Bus Interface Unit 70 and Intermodule Bus 72 (FIG. 2).

In operation, if the Left/Right Justify Control bit is a first value, e.g. a logical "1", transmission gates 150-165 will be turned ON, transmission gates 150'-165' will be turned OFF, and consequently the 10-bit result word RESULT[0]-RESULT[9] will be gated out in a left-justified format through DATA[6]-DATA[15].

On the other hand, if the Left/Right Justify Control bit is a logical "0", transmission gates 150-165 will be turned OFF, transmission gates 150'-165' will be turned ON, and consequently the 10-bit result word RESULT[0]-RESULT[9] will be gated out in a right-justified format through DATA[0]-DATA[9].

The sign control is determined by the logical state of the Sign Control signal over line 130 and by the Left/-Right Justify Control signal 132.

The desired data result format may also be specified by host system software loading appropriate control information into the QADC module. For example, for-

mat information could be loaded (in the form of one or more bits in a CCW or control register) to specify the desired data result format for each conversion, for a scan sequence or group of conversions, for each channel (as one or more control register bits per pin), or for a group of channels.

ALTERNATIVE EMBODIMENTS

It will be apparent to one of ordinary skill that the present invention can be implemented in many different ways.

For example, the system architecture could be arranged differently. The bus structure to the host processor could be different. The control word queues and result registers could be coupled to the host processor bus rather than associated with the QADC module.

The various control words, tables, and registers could contain more or fewer number of bits and data fields, and they could be arranged in many other ways. The register addresses and bit assignments could be altered.

The control fields can be implemented in different control words. For instance, the MUX field in Control Word 0 could be implemented within a different control word, such as the Module Configuration word in Module Configuration Register (FIG. 6).

The CCW table 62 could be a ROM. It could also be a single register storing a CCW containing control information to control the desired conversion process, e.g. all channels in a specified sequence.

The number of input analog pins could be fewer or more. The number of channels could be expanded by employing a larger channel field (CHAN) in the CCW. Pin assignments and functions and channel numbers (FIG. 9) could be altered.

The converter resolution could include more or fewer bits or could be selectable via a data field in a control word.

The queue lengths could be longer or shorter, and there could be more or fewer queues, including a queue only one CCW long. There could be more or fewer queue-initiating modes on each queue. There are a variety of ways for identifying the beginning and end of each queue.

There could be fewer or more data result formats, and, as mentioned above, there are a variety of other ways to select which data result format applies to each conversion, group of conversions, channel, or group of channels.

All of the conversion initiation methods (external trigger, periodic interval, continuous, software initiated), and most of the rest of the QADC features, can be applied to an A/D module that does not use a CCW queue to schedule the channels to be converted.

There can be more or less versatility regarding the selection of the input sample time.

There are other ways to convert two simultaneously sampled channels, and the selection of which channels and how many channels are to be sampled simultaneously can be more or less versatile.

The selection of which reference pins are to be used can be more or less versatile.

The power pins, reference pins, external trigger pins, and external MUX interface pins could be separate or shared with the analog input signals. The MUX addressing signals and MUX analog inputs need not necessarily be transmitted on pins also functioning as analog input channels.

The number of external multiplexers could be altered. Other variations to the module definition could affect the MUX function.

The channel selection need not be performed by a CCW in a queue. A sequential scan of the channel numbers could also be used.

Control signals in addition to the MUX addressing signals used in the Queued A/D Converter module could also be used, such as an "enable" signal on an external MUX.

The interrupt structure could be less or more versatile. For example, instead of restarting the lower priority queue at its beginning after the higher priority queue has completed its conversion sequence, the lower priority queue could be resumed with the next CCW in its sequence.

The clock source and prescaler selection could be more or less versatile.

The periodic timer rate selection could be more or less versatile, and there could be more than one selectable rate.

The external trigger could originate from another module of the same I.C. It need not be an external pin.

The CCW (FIG. 7) could contain more or fewer parameters to specify the characteristics of each sample, hold, and conversion.

One or more bits in each CCW could be utilized to designate the data format. For example, bits could be provided for resolution (result size) or for result data format, such as left/right justification and signed/unsigned data.

In addition, one or more bits in each CCW could be utilized to designate the sample time.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:

1. An analog-to-digital conversion system comprising:
   (a) at least one analog input terminal;
   (b) means for reading at least one command word, said command word designating an input sample time;
   (c) means responsive to said reading means for sampling an analog signal on said at least one analog input terminal for the duration of said input sample time; and
   (d) analog-to-digital converter means responsive to said sampling means for converting the sampled value of said analog signal into a digital value.

2. The analog-to-digital conversion system recited in claim 1 and comprising a plurality of analog input terminal, wherein said input sample time is specified for each of said terminals.

3. The analog-to-digital conversion system recited in claim 1 and comprising a plurality of analog input terminals, wherein a single input sample time is specified for said plurality said terminals.

4. The analog-to-digital conversion system recited in claim 1, wherein said analog-to-digital conversion system is on an integrated circuit.

5. An analog-to-digital conversion system comprising:
   (a) at least one analog input terminal;
   (b) means for reading at least one command word, said command word designating an input sample time;

(c) means responsive to said reading means for sampling an analog signal on said at least one analog input terminal for the duration of said input sample time; and

(d) analog-to-digital converter means responsive to said sampling means for converting the sampled value of said analog signal into a digital value; and

(e) means for repeating said sampling a predetermined number of times.

6. The analog-to-digital conversion system recited in claim 5, wherein the same input sample time is used for each sampling.

7. The analog-to-digital conversion system recited in claim 5, wherein an input sample time is specified for each sampling.

8. The analog-to-digital conversion system recited in claim 5 and comprising a plurality of analog input terminals, wherein said input sample time is specified for each successive sampling for each of said terminals.

9. The analog-to-digital conversion system recited in claim 5 and comprising a plurality of analog input terminals, wherein said input sample time is specified for each successive sampling of said plurality of terminals as a whole.

10. The analog-to-digital conversion system recited in claim 5 and comprising a plurality of analog input terminals, wherein the same input sample time is specified for each successive sampling of said plurality of terminals as a whole.

11. The analog-to-digital conversion system recited in claim 5, wherein said converter means converts each sampled value of said analog signal into a digital value.

12. The analog-to-digital conversion system recited in claim 5, wherein said analog-to-digital conversion system is on an integrated circuit.

13. An analog-to-digital conversion system comprising:

(a) a plurality of analog input terminals;

(b) means for reading a plurality of command words, at least one of said command words designating an input sample time;

(c) means responsive to said reading means for sampling an analog signal on each of said analog input terminals for the duration of said input sample time; and

(d) analog-to-digital converter means responsive to said sampling means for converting the sampled values of said analog signals into digital values.

14. The analog-to-digital conversion system recited in claim 13, wherein said plurality of command words defines at least one queue.

15. The analog-to-digital conversion system recited in claim 13, wherein said plurality of command words comprises a first queue and a second queue.

16. The analog-to-digital conversion system recited in claim 13, wherein said sampling means is responsive to said at least one command word to repetitively sample an analog signal on one of said plurality of input terminals for the duration of said input sample time.

17. The analog-to-digital conversion system recited in claim 13, wherein said input sample time is specified for each successive sampling for each of said terminals.

18. The analog-to-digital conversion system recited in claim 13, wherein said input sample time is specified for each successive sampling of said plurality of terminals as a whole.

19. The analog-to-digital conversion system recited in claim 13, wherein the same input sample time is specified for each successive sampling of said plurality of terminals as a whole.

20. An analog-to-digital conversion system comprising:

(a) a plurality of analog input terminals;

(b) means for reading a plurality of command words, each of said command words designating an input sample time for a corresponding input terminal;

(c) means responsive to said reading means for sampling an analog signal on each of said analog input terminals for the duration of said corresponding input sample time; and

(d) analog-to-digital converter means responsive to said sampling means for converting the sampled values of said analog signals into digital values.

21. The analog-to-digital conversion system recited in claim 20, wherein said plurality of command words defines at least one queue.

22. The analog-to-digital conversion system recited in claim 20, wherein said plurality of command words comprises a first queue and a second queue.

23. A method of converting an analog signal into a digital signal, said method utilizing a conversion system comprising at least one analog input terminal, means for reading at least one command word, said command word comprising information designating an input sample time, means for sampling an analog signal on said at least one analog input terminal, and analog-to-digital converter means for converting the sampled value of said analog signal into a digital value, said method comprising the steps of:

(a) reading said at least one command word; and

(b) responsive to said at least one command word, sampling an analog signal on said at least one analog input terminal for the duration of said input sample time.

24. A method of converting an analog signal into a digital signal, said method utilizing a conversion system comprising a plurality of analog input terminals, means for reading a plurality of command words, each of said command words comprising information designating an input sample time, means for sampling an analog signal on said analog input terminals, and analog-to-digital converter means for converting the sampled values of said analog signals into digital values, said method comprising the steps of:

(a) reading one of said command words; and

(b) responsive to said command word, sampling an analog signal on one of said analog input terminals for the duration of said input sample time.

25. The method recited in claim 24 and further comprising:

(c) repeating steps (a) and (b) for each of said plurality of input terminals.

26. The method recited in claim 24 and further comprising:

(d) repeating steps (a) and (b) for more than one sample of one of said input terminals.

27. A method of converting an analog signal into a digital signal, said method utilizing a conversion system comprising a plurality of analog input terminals, means for reading a plurality of command words, each of said command words comprising information designating an input sample time, means for sampling an analog signal on said analog input terminals, and analog-to-digital converter means for converting the sampled values of said analog signals into digital values, said method comprising the steps of:

(a) reading one of said command words; and

(b) responsive to said command word, sampling an analog signal on all of said analog input terminals for the duration of said input sample time.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,081,454

DATED : 01/14/92

INVENTOR(S) : Jules D. Campbell, Jr. et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 26, lines 53-54, change "terminal" to "terminals"

Signed and Sealed this

Seventh Day of September, 1993

Attest:

Attesting Officer

BRUCE LEHMAN

Commissioner of Patents and Trademarks

Exhibit D

US005089722A

United States Patent [19]

Amedeo

[11] Patent Number: 5,089,722

[45] Date of Patent: Feb. 18, 1992

[54] **HIGH SPEED OUTPUT BUFFER CIRCUIT WITH OVERLAP CURRENT CONTROL**

[75] Inventor: **Robert J. Amedeo**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **503,012**

[22] Filed: **Apr. 2, 1990**

[51] **Int. Cl.**[5] **H03K 17/16**; H03K 19/094; H03K 5/12; H03K 17/687

[52] **U.S. Cl.** **307/443**; 307/451; 307/542; 307/475; 307/548; 307/558; 307/263

[58] **Field of Search** 307/270, 443, 542, 572, 307/448, 451, 452, 585, 552, 555, 558, 568, 592, 594, 597, 246, 263, 242, 475, 547, 548

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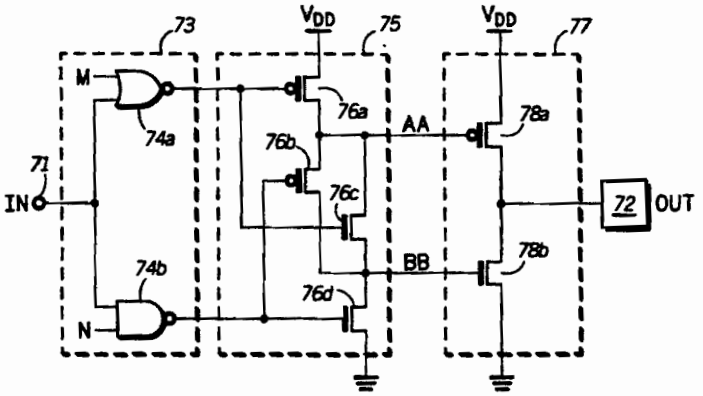
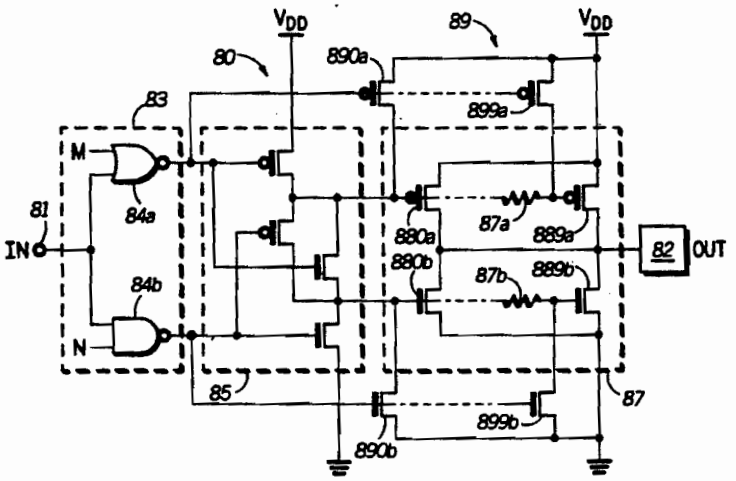
Primary Examiner—Edward P. Westin
Assistant Examiner—David R. Bertelson
Attorney, Agent, or Firm—Robert L. King

[57] **ABSTRACT**

A pre-driver stage includes two pairs of series-stacked transistors for responding to input stage outputs and provides first and second outputs to an output driver stage. The first output becomes low at a certain delay period after the second output becomes low, and the second output becomes high at a certain delay period after the first output becomes high. Therefore, the turn-off of the active driver transistor is completed before the turn-on of the opposite output transistor, inhibiting an overlap current. In another form, the buffer circuit also uses assist transistors placed near the driver transistors for assisting the oppsoite driver transistors in turning off.

14 Claims, 4 Drawing Sheets





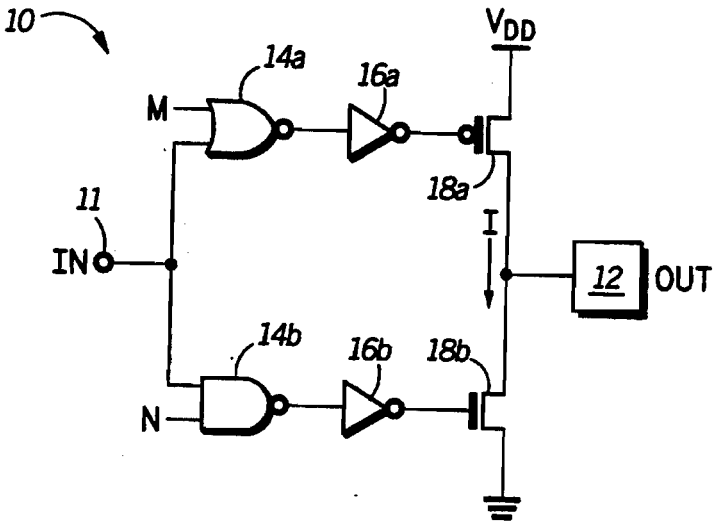


FIG. 1A
-PRIOR ART-

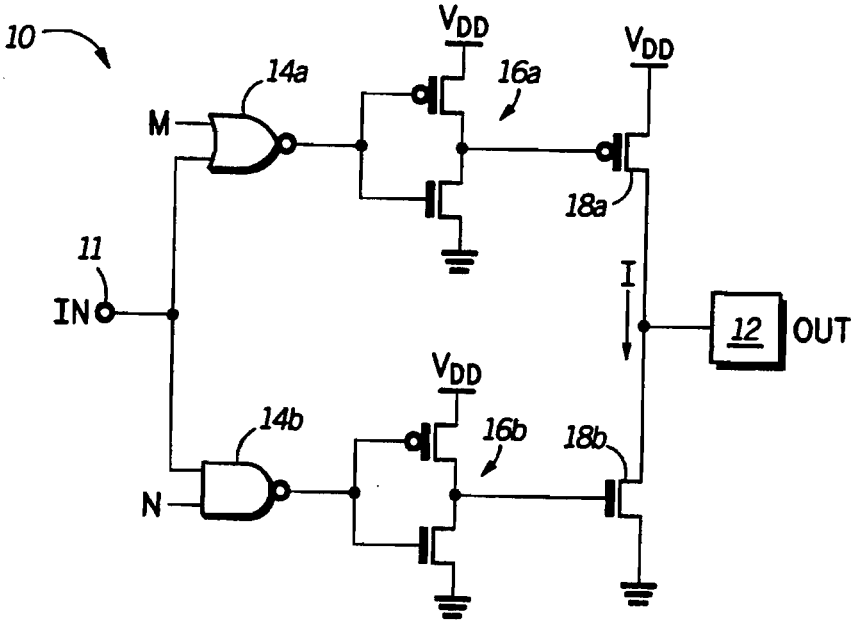


FIG. 1B
-PRIOR ART-

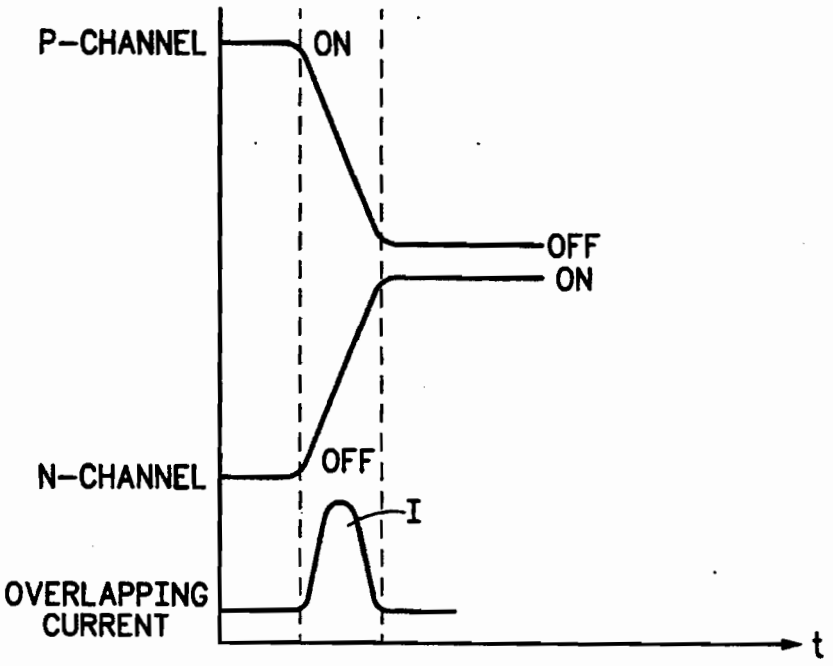


FIG.2

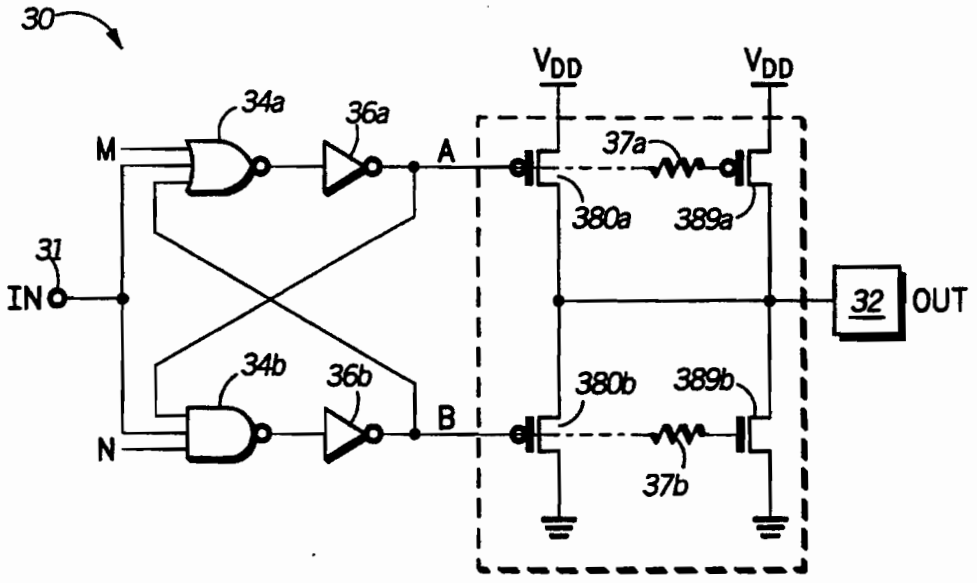


FIG.3
-PRIOR ART-

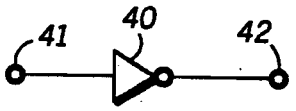


FIG.4A

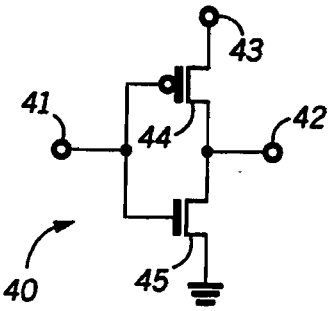


FIG.4B

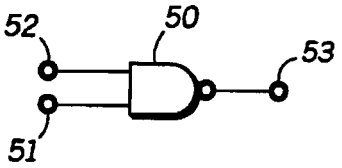


FIG.5A

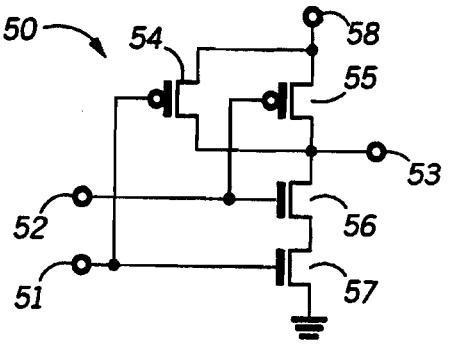


FIG.5B

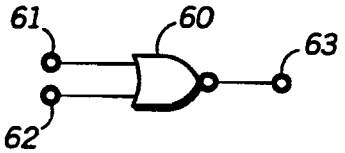


FIG.6A

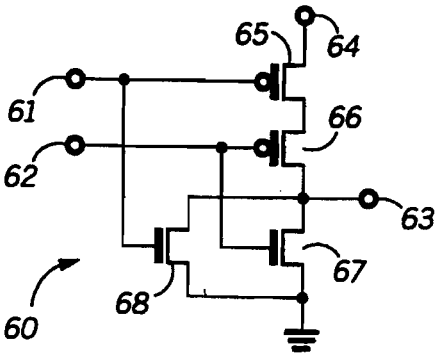
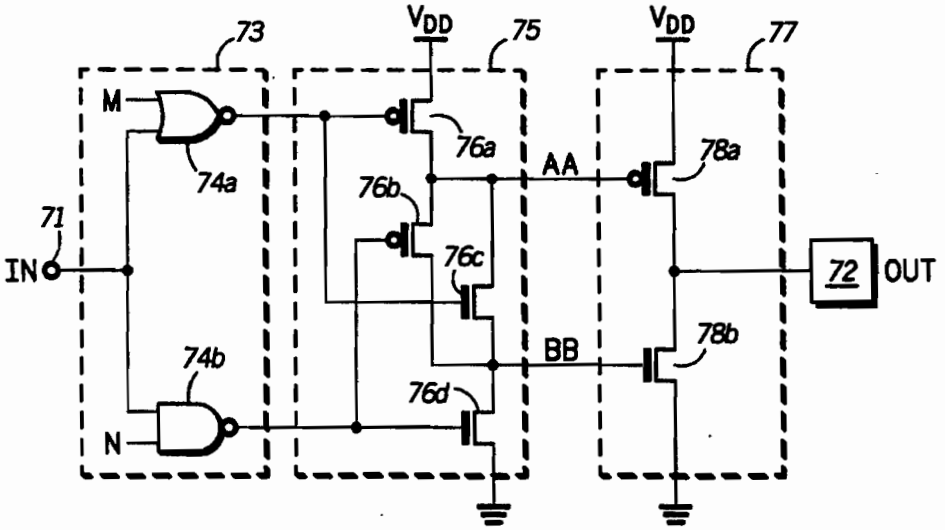


FIG.6B


73
V_{DD}
75
V_{DD}
77
M
74a
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AA
78a
71
IN
76b
76c
72
OUT
74b
BB
78b
76d
N

FIG. 7

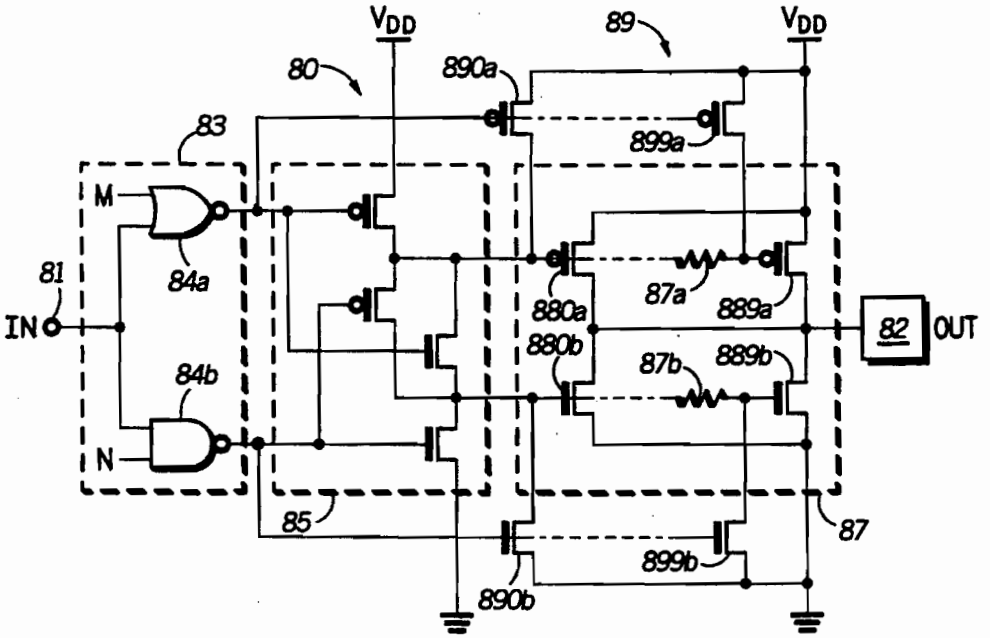
V_{DD}
89
V_{DD}
80
890a
899a
83
M
84a
87a
81
IN
880a
889a
82
OUT
880b
87b
889b
84b
N
85
87
899b
890b

FIG. 8

HIGH SPEED OUTPUT BUFFER CIRCUIT WITH OVERLAP CURRENT CONTROL

FIELD OF THE INVENTION

The present invention relates, in general, to an output buffer circuit. More particularly, the invention relates to a CMOS (complementary metal-oxide-silicon) output buffer circuit with high speed switching and large power handling capacity.

BACKGROUND OF THE INVENTION

Many digital output or driver circuits have been developed for use in MOS FET(field effect transistor) integrated circuitry, especially for use at output pads (terminals) of microprocessors or microcomputers. A CMOS output buffer having a complementary pair of transistors in an output stage is widely used and operates at a relatively high speed and reduces the internal power consumption when the buffer is in one or the other of its two logic states. However, the basic CMOS output buffer has a disadvantage that an overlapping current passes through the P-channel and N-channel transistor of the output stage in the buffer when it is switching from one logic state to the other.

In addition, it is desirable that the conventional buffer circuit be able to source (and sink) a large amount of current to (and from) external circuitry connected thereto. But, it is difficult to drive external large circuit loads by the conventional CMOS output buffer.

Attempts to overcome such defects of the single transistor pair CMOS output buffer include cross-coupling pre-drivers with input logic gates to provide propagation delays. Others have also connected multiple complementary transistor pairs in parallel in an output stage to increase the source and sink currents. However, such cross-coupling buffer circuits require additional interconnections which undesirably increase the complexity of the circuit, and the propagation delay period of the circuit cannot be controlled. Further, the multiple complementary transistor pair output buffer worsens the overlapping current problem, as described below in detail.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved output buffer circuit which has high switching speed with overlap current control.

More particularly, it is an object of the present invention to provide an improved output buffer circuit having large power driving capacity with overlap current control.

Yet another object of the present invention is to provide an improved output buffer circuit which can be easily implemented into existing circuits without additional process steps or area.

In carrying out the above and other objects of the invention there is provided, in one form, an output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal. The output buffer circuit comprises an input stage, a pre-driver stage, and an output driver stage having a pair of driver transistors connected in series. The pre-driver stage includes two pairs of stacked transistors for responding to the input stage outputs and provides first and second outputs to the output driver stage. The first output assumes a first logic state after a first predetermined controlled delay period after the second output assumes the first logic state, and the second output assumes a second logic state after a second predetermined controlled delay period after the first output assumes the second logic state. The turn-off of an active driver transistor in the driver stage is completed before the turn-on of a second driver transistor in the driver state, thereby preventing an overlap current.

According to another feature of the invention, the output buffer circuit further comprises assist semiconductor devices placed near the corresponding driver transistors for assisting the driver transistors in turning off.

These and other objects, features, and advantages, will be more clearly understood from the detailed description below together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a partial schematic diagram of a known output buffer circuit having a basic CMOS driver;

FIG. 1B shows the circuit of FIG. 1A, illustrating the inverters schematically;

FIG. 2 is a graph illustrating the generation of an overlap current in an output driver;

FIG. 3 is a partial schematic diagram of another known output buffer circuit having a cross-coupling structure;

FIGS. 4A and 4B show, respectively, the symbol of an inverter and its schematic diagram when implemented utilizing MOS transistors;

FIGS. 5A and 5B show, respectively, the symbol for a NAND gate and its schematic diagram utilizing MOS transistors;

FIGS. 6A and 6B show, respectively, the symbol for a NOR gate and its schematic diagram utilizing MOS transistors;

FIG. 7 is a schematic diagram of one embodiment of an output buffer circuit of this invention; and

FIG. 8 is a schematic diagram of another embodiment of an output buffer circuit of this invention.

DETAILED DESCRIPTION OF THE INVENTION

As mentioned before, although a conventional basic CMOS output buffer has the advantage of low quiescent current, it also has a disadvantage of an overlap current when switching between logic states. First, a brief reference will be made to a basic CMOS output buffer.

FIG. 1A schematically shows an example of a known CMOS output buffer. As shown in FIG. 1A, a basic output buffer circuit 10 includes a data input terminal 11 for receiving a data logic signal IN, and an output signal terminal 12 for providing an output logic signal OUT to external circuitry (not shown). When buffer 10 is receiving a logically high signal at terminal 11, the logic high signal is applied to a first input of a NOR gate 14*a*, thereby causing NOR gate 14*a* to provide a logic low signal on its output lead which is connected to the input of an inverter 16*a*. The logic state of an enable signal M connected to a second input of NOR gate 14*a* is assumed to be a logic low. Inverter 16*a* supplies at an output a logic high output signal which is applied to the gate of a P-channel MOS (metal-oxide-silicon) FET (field effect transistor) 18*a*, thus making P-channel transistor 18*a* nonconductive.

Simultaneously, the logic high signal at input terminal 11 is applied also to a first input of a NAND gate 14*b* with a second input receiving a logic high enable signal N, thereby causing NAND gate 14*b* to provide a logic low signal at its output which is connected to the input of an inverter 16*b*. Inverter 16*b* supplies on its output a logic high output signal which is applied to the gate of an N-channel MOS transistor 18*b*, thus making N-channel transistor 18*b* conductive.

In this way, with buffer 10 receiving a logic high data signal, P-channel transistor 18*a* is off (nonconductive) and N-channel transistor 18*b* is on (conductive), thus effectively connecting output signal terminal 12 to ground through N-channel transistor 18*b* and disconnecting output signal terminal 12 from the positive supply voltage V_{DD}. Therefore, a logic low output signal is provided and buffer 10 is allowed to sink current from external circuitry (not shown) connected to terminal 12.

Conversely, when buffer 10 is receiving a logic low input signal, the logic low input signal is applied to the first input of NOR gate 14*a* with the second input thereof receiving a logic low enable signal M, thereby causing NOR gate 14*a* to provide a logic high signal at its output which is connected to the input of inverter 16*a*. Inverter 16*a* supplies at its output a logic low output signal which in turn is applied to the gate of P-channel transistor 18*a*, thus making P-channel transistor 18*a* conductive.

Simultaneously, the logic low signal at input terminal 11 is applied also to the first input of NAND gate 14*b* with the second input thereof still receiving a logic high enable signal N, thereby causing NAND gate 14*b* to provide a logic high at its output which is connected to the input of inverter 16*b*. Inverter 16*b* supplies at its output logic low output signal which in turn is applied to the gate of N-channel transistor 18*b*, thus making N-channel transistor 18*b* nonconductive.

In this manner, with buffer 10 receiving a logic low data signal, output signal terminal 12 is effectively connected to positive supply voltage V_{DD} and is disconnected from ground, therefore providing a logic high output signal and allowing buffer 10 to source current to external circuitry (not shown).

However, in this basic CMOS output buffer 10, because each signal from inverters 16*a* and 16*b* respectively arrives at the gates of transistors 18*a* and 18*b* simultaneously, P-channel transistor 18*a* turns off and N-channel transistor 18*b* turns on at the same time, as shown by a graph in FIG. 2, and vice versa. That is, the period of transient logic state of transistor 18*a* overlaps with the transient period of transistor 18*b*. Therefore, during the transient periods of transistors 18*a* and 18*b*, a current I passes from supply voltage V_{DD} through transistors 18*a* and 18*b* to ground. This overlap current (sometimes called "spike current") is especially high in a large output buffer having high power driving capability. The overlap current I is undesirable because it increases internal current consumption and causes RFI (radio frequency interference) which adversely affects other circuitry.

FIG. 3 shows another example of another known output buffer designed to solve the overlap current problem. As shown in FIG. 3, a cross-coupled output buffer circuit 30 includes a data input terminal 31 for receiving a digital data input signal IN, and an output signal terminal 32 for providing an output signal OUT to external circuitry (not shown). Output buffer 30 also includes a predetermined number of pairs of P-and N-channel MOS transistors 380*a, b* through 389*a, b* as noted by the dashed lines. Input terminal 31 is connected to a first input of a NOR gate 34*a* and to a first input of a NAND gate 34*b*. The output of each of NOR gate 34*a* and NAND gate 34*b* is connected to an input of inverters 36*a* and 36*b*, respectively. Output signals A and B from inverters 36*a* and 36*b*, respectively, are applied to the gates of multiple P-channel and N-channel transistors 380*a* through 389*a* and 380*b* through 389*b*, respectively. The circuit structure of cross-coupled buffer 30 is almost the same as that of CMOS buffer 10 shown in FIG. 1A, except that the output leads of inverters 36*a* and 36*b* are cross-coupled to other inputs of the NAND gate 34*b* and NOR gate 34*a* respectively, as shown in FIG. 3.

When buffer 30 is receiving a logic high data input signal, P-channel transistors 380-9*a* are off and N-channel transistors 380-9*b* are on, thus effectively connecting output signal terminal 32 to ground through N-channel transistors 380-9*b* and disconnecting output signal terminal 32 from a positive supply voltage V_{DD}. Therefore a logic low output signal is provided and buffer 30 is allowed to sink a large amount of current from external circuitry (not shown) connected to terminal 32.

Conversely, when buffer 30 is receiving a logic low data input signal, output signal terminal 32 is effectively connected to positive supply voltage V_{DD} and is disconnected from ground, therefore providing a logic high output signal and allowing buffer 10 to source a large amount of current to the external circuitry.

When the data input signal IN changes from one logic state to the other, the transient behaviors of output signals A and B respectively from inverters 36*a*, 36*b* are different from the outputs of inverters 16*a* and 16*b* of buffer 10 shown in FIG. 1A.

When the data input signal IN changes from logic high to logic low, the output of NAND gate 34*b* changes from low to high after one NAND gate delay. Then output signal B of inverter 36*b* changes from high to low after one inverter delay, and thereafter turns off each of N-channel transistors 380-9*b*. On the other hand, when data input signal IN changes from high to low, all inputs of NOR gate 34*a* do not change to low at once. A cross-coupled second input of NOR gate 34*a* which is provided with output signal B by inverter 36*b* slowly changes to low after one NAND gate and one inverter gate delay. After that, output signal A of inverter 36*a* changes to low after one NOR gate and one inverter gate delay, and then turns on P-channel transistors 380-9*a*. Therefore, the turn-on of P-channel transistor 380*a* is delayed after the turn-off of N-channel transistor 380*b* by one NOR gate and one inverter gate delay period, thereby inhibiting overlap current.

Conversely, when data input signal IN changes from low to high, the turn-on of N-channel transistor 380*b* is delayed after the turn-off of P-channel transistor 380*a* by one NAND gate and one inverter gate delay period, to inhibit overlap current.

However, this cross-coupled output buffer 30 also has disadvantages. The delay period resulting from the cross-coupling is too long due to plural transistor feedback gates (explained below in more detail), and cannot be accurately controlled.

In the case where multiple complementary transistor pairs 380-9*a, b* are employed, the last transistors 389*a, b* turn off much later, because parasitic impedance such as resistances 37*a, b* exist between the gate of the first transistor 380*a, b* and the gate of the last transistor 389*a,*

b. The parasitic impedance typcially results, in part, from the nature of the physical layout implementation of buffer **30** which is often required to comply with certain rules, in part, to control the conventional and well documented di/dt problem. Due to the delay of the turn-off of the last transistors **389***a, b*, electrical currents pass, for example, through P-channel transistor **389***a* and N-channel transistor **380***b* during the transient periods. Accordingly, in order to eliminate such cross-flowing overlap currents, more delay of the turn-on of the transistors is required and therefore more transistors are needed to accomplish the more delay. However these transistors are expensive and difficult to install, and their delay can not be adequately controlled.

Now, reference will be made to the inside structures of an inverter, a NAND gate and a NOR gate. An inverter, such as inverters **16***a, b* shown in FIG. **1**A, is comprised of two MOS transistors as shown in FIGS. **4**A and **4**B. FIG. **4**A shows the symbol for an inverter **40** having an input terminal **41** and an output terminal **42**. FIG. **4**B shows the MOS transistor implementation of the inverter **40**. As shown in FIG. **4**B, inverter **40**, again having input terminal **41** and output terminal **42**, is constructed by suitably connecting a P-channel MOS transistor **44** and an N-channel MOS transistor **45**, with a terminal **43** being connected to a positive supply voltage. Thus, inverter **40** requires two MOS transistors. Therefore it should be understood that the circuit of FIG. **1**B is equivalent to buffer circuit **10** shown in FIG. **1**A.

Similarly, a three-input NAND gate, such as NAND gate **34***b* of FIG. **3**, requires six MOS transistors. A two-input NAND gate requires four transistors. As shown in FIGS. **5**A and **5**B, NAND gate **50**, having inputs **51** and **52** and an output **53**, is constructed utilizing P-channel MOS transistors **54** and **55**, and N-channel MOS transistors **56** and **57**, with a terminal **58** being connected to a positive supply voltage. Furthermore, a three-input NOR gate, such as NOR gate **34***a* of FIG. **3**, requires at a minimum four MOS transistors. As shown in FIGS. **6**A and **6**B, two-input NOR gate **60**, having inputs **61** and **62** and an output **63**, is constructed utilizing P-channel MOS transistors **65** and **66**, and N-channel MOS transistors **67** and **68**.

Accordingly it should be understood that the propagation delay of NOR gate **34***a* of FIG. **3** is equal to two transistor gate delays when its output changes low to high. And it also should be understood that the propagation delay of NAND gate **34***b* of FIG. **3** is equal to two transistor gate delays when its output changes high to low.

In FIG. **3**, when data input signal IN changes high to low, the turn-on of P-channel transistor **380***a* is delayed after the turn-off of N-channel transistor **380***b* by three transistor gate delay periods, which is too long and uncontrollable. Conversely, when data input signal IN changes from low to high, the turn-on of N-channel transistor **380***b* is delayed after the turn-off of P-channel transistor **380***a* by three transistor gate delay periods, which is also too long and uncontrollable.

The output buffer circuit according to the present invention will now be described in detail with reference to preferred embodiments thereof, which are illustrated in FIGS. **7** and **8**.

For convenience of explanation, certain transistor gates are specifically described as P-channel or N-channel. However, those of skill in the art will understand that theses are merely for ease of explanation and not intended to be limiting, and that the present invention includes arrangements where the channel types are inverted and/or where other combinations of P- and N-channels and voltage polarities are used. As is well understood, the FET devices of the circuit as well as other circuit components and their interconnections as illustrated may be fabricated as an integrated circuit in a single body of semiconductor material.

As shown in FIG. **7**, an output buffer circuit **70** includes a data input terminal **71** for receiving a data input signal IN, an output signal terminal **72** for providing an output signal OUT, an input stage **73**, a pre-driver stage **75**, and an output driver stage **77**. Input stage **73** comprises a NOR gate **74***a* and a NAND gate **74***b*. One input lead of NOR gate **74***a* and one input lead of NAND gate **74***b* are connected in common to receive the data input signal IN from input terminal **71**. Other input leads of both gates **74***a, b* are used for receiving control or enable signals (not shown).

Pre-driver stage **75** comprises a first stacked pair of P-channel MOS FETs **76***a* and **76***b*, and a second stacked pair of N-channel MOS FETs **76***c* and **76***d*. P-channel transistors **76***a* and **76***b* are serially connected between a supply voltage V_{DD} and a juncture of serially connected N-channel transistors **76***c* and **76***d*. N-channel Transistors **76***c* and **76***d* are serially connected between ground and a juncture of P-channel transistors **76***a* and **76***b*. The output of NOR gate **74***a* is connected to the gates of P-channel transistor **76***a* and N-channel transistor **76***c*. The output of NAND gate **74***b* is connected to the gate of P-channel transistor **76***b* and N-channel transistor **76***d*. A first output AA of pre-driver stage **75** is derived at a node between P-channel transistors **76***a* and **76***b*. A second output BB of pre-driver stage **75** is derived at a node between N-channel transistors **76***c* and **76***d*.

It should be noted that pre-driver stage **75** has the same number of transistors as buffer circuit **10** of FIGS. **1**A and **1**B. That is, implementation of pre-driver stage **75** can be accomplished by using the same number of transistors as in the known circuit but rewiring them as shown in FIG. **7**.

Output driver stage **77** comprises a complementary pair of a P-channel MOS FET **78***a* and an N-channel MOS FET **78***b*. The MOS FETs **78***a* and **78***b* are connected in series between voltage supply V_{DD} and ground. The gate of P-channel MOS FET **78***a* receives output AA from pre-driver stage **75**. The gate of N-channel MOS FET **78***b* receives output BB from pre-driver stage **75**. The output signal OUT is derived at a juncture of MOS FETs **78***a* and **78***b*.

In operation, when data input signal IN at input terminal **71** changes from logic low to high, the logic high signal is applied to a first input of NOR gate **74***a* thereby causing NOR gate **74***a* to generate a logic low signal at its output which is connected to the gates of transistors **76***a* and **76***c*. An enable signal M is at a logic low. Thus, P-channel transistor **76***a* turns on (conductive) and N-channel transistor **76***c* turns off (nonconductive), thus changing output AA to high immediately. High output AA is applied to the gate of P-channel transistor **78***a*, thus causing P-channel transistor **78***a* to turn off.

Simultaneously, the logic high input signal IN is applied also to a first input of NAND gate **74***b* with the other input lead receiving a logic high enable signal N, thereby causing NAND gate **74***b* to provide a logic low signal at its output which is connected to the gates of transistors **76***b* and **76***d*. Thus, P-channel transistor **76***b*

turns on and N-channel transistor 76*d* turns off. Output BB becomes high at a delay period after output AA becomes high. This is because two stacked transistors 76*a* and 76*b* must turn on thereby providing output BB as a logic high while transistor 76*a* must turn on for output AA to be a logic high.

Therefore, N-channel transistor 78*b* does not become conductive until P-channel transistor 78*a* is completely nonconductive, thereby inhibiting overlap current. This delay period is determined by the sizes, especially the width-to length ratios (W/L), of transistors 76*a*, 76*b*; therefore it can be controlled.

Conversely, when data input signal IN at input terminal 71 changes from a logic high to low, the logic low signal is applied to the first input of NAND gate 74*b* thereby causing NAND gate 74*b* to generate a logic high signal at its output which is connected to the gates of transistors 76*b* and 76*d*. Thus, N-channel transistor 76*d* turns on and P-channel transistor 76*b* turns off, thereby changing output BB immediately to a logic low. Logic low output BB is applied to the gate of N-channel transistor 78*b*, thus causing N-channel transistor 78*b* to turn off.

Simultaneously, the logically low input signal IN is applied also to the first input of NOR gate 74*a* with the second input receiving a low enable signal M, thereby causing NOR gate 74*a* to generate a logic high signal on its output which is connected to the gates of transistors 76*a* and 76*c*. Thus, P-channel transistor 76*a* turns off and N-channel transistor 76*c* turns on. Output AA becomes low at a delay period after output BB becomes low. This is because two stacked or series-connected transistors 76*c* and 76*d* must turn on to provide a low output AA while only one transistor 76*d* must turn on for a low output BB.

Therefore, P-channel transistor 78*a* does not become conductive until N-channel transistor 78*b* is completely shut off, thereby inhibiting the overlap current. This delay period is determined by the transistor sizes, especially the width-to length ratios (W/L), 76*c*, 76*d*; therefore the delay can be controlled. That is, the transient period of transistor 78*a* does not overlap with the transient period of transistor 78*b*. Thus output buffer circuit 70 provides no or significantly reduced overlap current and less noise by turning off the active output transistor before turning on the opposing output transistor. By controlling the width-to length ratios (W/L) of transistors in pre-driver stage 75, the delay period can be very easily controlled. This pre-driver structure can be easily retrofit into existing output buffer designs.

FIG. 8 shows another embodiment according to the present invention. An output buffer circuit 80 includes a data input terminal 81 for receiving an input data signal IN, an output signal terminal 82 for providing an output signal OUT, an input stage 83, a pre-driver stage 85, and an output driver stage 87. The circuit structure of output buffer 80 of this embodiment is almost the same as that of the first embodiment buffer 70 shown in FIG. 7 except that output driver stage 87 includes a predetermined number of plural pairs of P-channel and N-channel MOS transistors 880*a*, *b* through 889*a*, *b*, as noted by the dashed lines. Output buffer 80 further comprises assist transistors 89.

In the illustrated form, assist transistors 89 include P-channel MOS FETs 890*a* through 899*a*, and N-channel MOS FETs 890*b* through 899*b*. P-channel transistor 899*a*, for example, is placed near the gate of corresponding P-channel transistor 889*a* to enhance the turn-off of transistor 889*a*. Other assist transistors 890 through 899 are placed near the gates of corresponding transistors 880 through 889. The gate of P-channel transistor 899*a* is connected to an output of NOR gate 84*a*, its source is connected to a positive supply voltage V_{DD}, and its drain is connected to the gate of transistor 889*a*.

It should be apparent from the previous discussion that significant impedance such as parasitic resistance 87*a* exists between the gate of transistor 880*a* and transistor 889*a*. This impedance causes overlap currents by slowing down the turn-off of the opposite drivers, as described above with reference to FIG. 3. Assist transistor 899*a* compensates the slowing down of the turn-off of opposite transistor 889*a* caused by the impedance, and facilitates the quick turn-off of transistor 889*a*. Other assist transistors may be similarly connected and function similarly. Assist transistors 890*a*, *b* through 899*a*, *b* are responsible for the turn-off direction only.

In this way, the combination of the stacked pre-driver transistors and the assist devices provide a faster and quieter output buffer circuit relative to what is conventionally used in CMOS applications. The output buffer circuit according to the invention provides great reduction in overlap current, RFI noise and power consumption.

While the present invention has been shown and described with reference to particular embodiments thereof, various modifications and changes thereto will be apparent to those skilled in the art and are within the spirit and scope of the present invention.

I claim:

1. An output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal, comprising:

an input stage for receiving the data signal from the data input terminal and for providing input stage outputs;

a pre-driver stage for receiving the input stage outputs and for providing first and second outputs in response to the input stage outputs, said first output becoming logically low after a first predetermined controlled delay period after said second output becomes logically low, and said second output becoming logically high after a second predetermined controlled delay period after said first output becomes logically high; and

an output driver stage for receiving said first and second outputs from the pre-driver stage and for providing the output signal to the output signal terminal, said output driver stage including at least one complementary pair of serially connected output transistor devices, and said output signal being derived at a node between said serially connected output transistor devices,

said first and second outputs of the pre-driver stage being supplied only to said output driver stage and not to said input stage.

2. An output buffer circuit according to claim 1 wherein said input stage comprises a first logic gate and a second logic gate each having at least one input and an output, said inputs of the first and second logic gates being connected together for receiving the data signal.

3. An output buffer circuit according to claim 1 wherein said pre-driver stage comprises:

a first pair of transistors being serially connected between a first supply voltage terminal and said second output of the pre-driver stage, a node be-

tween said first pair of transistors being connected to said first output of the pre-driver stage; and

a second pair of transistors being serially connected between said first output of the pre-driver stage and a second supply voltage terminal, a node between said second pair of transistors being connected to said second output of the pre-driver stage.

4. An output buffer circuit according to claim 3 wherein control electrodes of said first and second pairs of transistors are connected to the input stage outputs.

5. An output buffer circuit according to claim 4 wherein said first pair of transistors are MOS transistors of a first conductivity, and said second pair of transistors are MOS transistors of a second conductivity.

6. An output buffer circuit according to claim 5 wherein said first conductivity is a p-type conductivity, and said second conductivity is an n-conductivity.

7. An output buffer circuit according to claim 3 wherein:

said first predetermined controlled delay period is determined by width-to-length ratios (W/L) of said second pair of transistors; and

said second predetermined controlled delay period is determined by width-to-length ratios (W/L) of said first pair of transistors.

8. An output buffer circuit according to claim 1 wherein:

said at least one complementary pair of output transistor devices comprises a p-channel MOS transistor and an n-channel MOS transistor.

9. An output buffer circuit according to claim 8 wherein:

a source of said p-channel MOS transistor is connected to a first supply voltage terminal;

a gate of said p-channel MOS transistor receives said first output from the pre-driver stage;

drain electrodes of both of said p-channel and n-channel MOS transistors are connected together for providing the output signal;

a gate of said n-channel MOS transistor receives the second output from the pre-driver stage; and

a source of said n-channel transistor is connected to a second supply voltage terminal.

10. An output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal, comprising:

an input stage for receiving the data signal from the data input terminal and for providing input stage outputs;

a pre-driver stage for receiving the input stage outputs and for providing first and second outputs in response to the input stage outputs, said first output becoming logically low at a first predetermined controlled delay period after said second output becomes logically low, and said second output becoming logically high at a second predetermined controlled delay period after said first output becomes logically high;

an output driver stage including a plurality of complementary pairs of serially connected p- and n-channel MOS transistors, said plurality of pairs being connected in parallel between first and second supply voltage terminals, control electrodes of said p-channel transistors receiving said first output from the pre-driver stage, control electrodes of said n-channel transistors receiving said second output from the pre-driver stage, and all nodes between said MOS transistors in said pairs being connected together for providing the output signal to the output signal terminal; and

assist means for receiving the input stage outputs and for assisting said MOS transistors in turning off,

said first and second outputs of the pre-driver stage being supplied only to said output driver stage and not to said input stage.

11. An output buffer circuit according to claim 10 wherein:

said input stage comprises a first logic gate and a second logic gate each having at least one input and an output, said inputs of the first and second logic gates being connected in common for receiving the data signal.

12. An output buffer circuit according to claim 10 wherein said pre-driver stage comprises:

a first pair of transistors being serially connected between a first voltage supply and said second output of the pre-driver stage, a node between said first pair of transistors being connected to said first output of the pre-driver stage; and

a second pair of transistors being serially connected between said first output of the pre-driver stage and a second voltage supply, a node between said second pair of transistors being connected to said second output of the pre-driver stage.

13. An output buffer circuit according to claim 12 wherein:

said assist means further comprise MOS transistors having gates connected to the input stage outputs, said assist means supplying signals for turning off the MOS transistors in the output driver stage.

14. An output buffer circuit according to claim 12 wherein:

said first predetermined controlled delay period is determined by width-to-length ratios (W/L) of said second pair of transistors; and

said second predetermined controlled delay period is determined by width-to-length ratios (W/L) of said first pair of transistors.

* * * * *

Exhibit E

US005105250A

United States Patent [19]

Tam et al.

[11] Patent Number: 5,105,250

[45] Date of Patent: Apr. 14, 1992

[54] **HETEROJUNCTION BIPOLAR TRANSISTOR WITH A THIN SILICON EMITTER**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **594,576**

[22] Filed: **Oct. 9, 1990**

[51] Int. Cl.[5] **H01L 29/72**; H01L 29/161; H01L 29/04

[52] U.S. Cl. **357/34**; 357/35; 357/16; 357/59

[58] Field of Search ..... 357/35, 34, 16, 59 H

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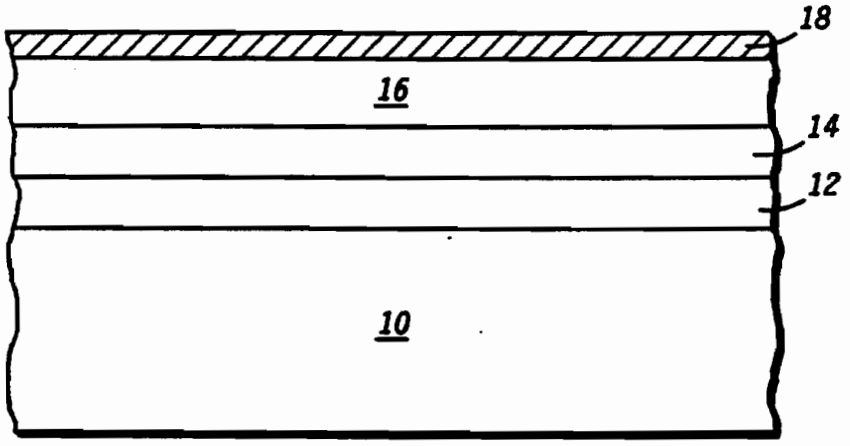
Assistant Examiner—Wael Fahmy
Attorney, Agent, or Firm—Miriam Jackson; Joe E. Barbee

[57] **ABSTRACT**

A heterojunction bipolar transistor having a thin, lightly doped, silicon emitter disposed on a silicon-germanium base layer exhibits low emitter resistance and low emitter-base capacitance. The lightly doped silicon emitter maintains the bandgap differential between silicon-germanium and silicon. The silicon emitter is fabricated such that the silicon emitter will be substantially depleted at zero bias, resulting in low emitter-base resistance and emitter resistance.

10 Claims, 1 Drawing Sheet



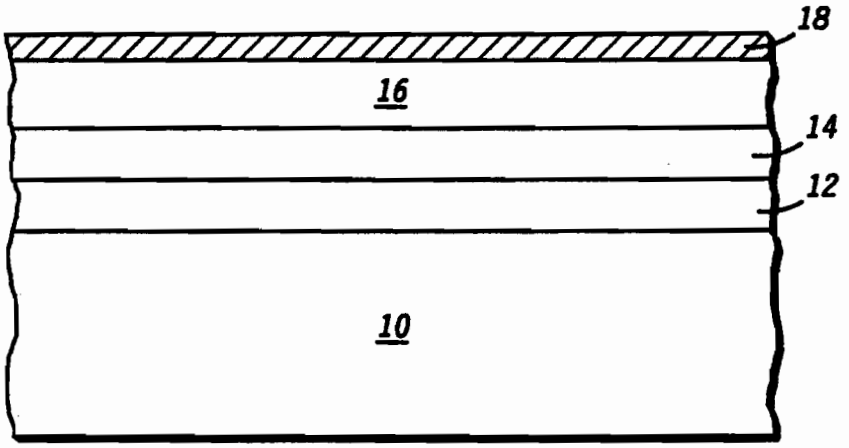
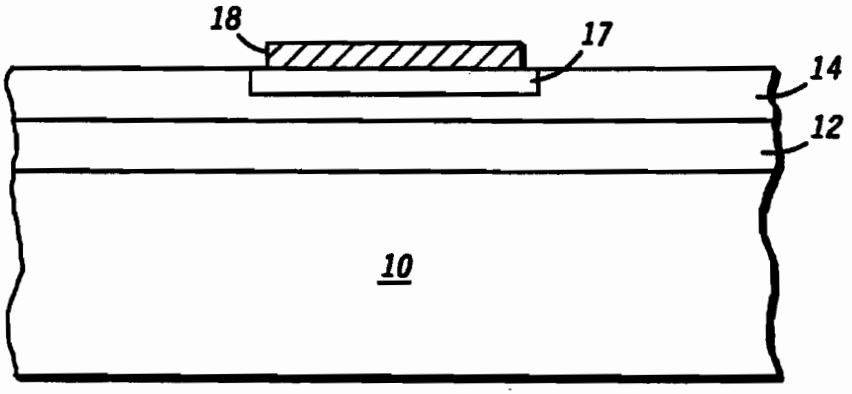


FIG. 1

FIG. 2



HETEROJUNCTION BIPOLAR TRANSISTOR WITH A THIN SILICON EMITTER

BACKGROUND OF THE INVENTION

This invention relates, in general, to semiconductor devices, and more particularly, to a heterojunction bipolar transistor.

Heterojunction bipolar transistors exhibit electrical characteristics which are advantageous over the electrical characteristics of homojunction bipolar transistors. Silicon-germanium heterojunction bipolar transistor processing is compatible with existing silicon processing. Thus, silicon-germanium heterojunction bipolar transistors are preferred over other heterojunction bipolar transistors. In particular, silicon-germanium heterojunction bipolar transistors exhibit high emitter injection efficiency, reduced charge storage in the emitter, reduced or eliminated hole injection into the emitter. These characteristics are obtained because of the bandgap differential between the silicon and silicon-germanium metallurgical junction.

A silicon-germanium heterojunction bipolar transistor of the prior art consists of an N-type silicon collector, a P-type silicon-germanium base, and an N-type polysilicon layer. The N-type dopant from the polysilicon is diffused into the base to form an emitter region. The problem with this structure is that boron diffuses into the polysilicon layer or arsenic diffuses into the silicon-germanium base during the formation of the emitter. This diffusion degrades the bandgap differential by moving the metallurgical junction from the silicon-germanium and polysilicon interface into either the polysilicon layer or into the silicon-germanium base. Thus, the advantageous electrical characteristics described above are not exhibited.

A way of maintaining the metallurgical junction at the silicon-germanium and polysilicon interface is to prevent the diffusion of boron or arsenic from the respective layers. A structure in which the polysilicon layer is used as the emitter would solve this problem because the diffusion of boron or arsenic can be prevented. However, in this structure, the interface between the polysilicon layer and the silicon-germanium layer is poor, which results in the transistor exhibiting poor electrical characteristics, such as high leakage.

A transistor which solves this interface problem has been disclosed by King et al, in an article entitled, "Si/-$Si_{1-x}Ge_x$ Heterojunction Bipolar Transistors Produced by Limited Reaction Processing," published in IEEE Electron Device Letters, Vol. 10, No. 2, on Feb. 1989. The use of a thick silicon emitter of approximately 4,000 angstroms in thickness, instead of the polysilicon emitter eliminates the interface problem, and maintains the bandgap differential between the silicon-germanium layer and the silicon emitter layer in this case. However, in this structure, the thick silicon emitter must be lightly doped to avoid breakdown voltage problems and to avoid high emitter-base capacitance. A lightly doped, thick emitter exhibits high emitter resistance. Thus, it would be desirable to fabricate a heterojunction bipolar transistor in which the bandgap differential is ensured and also where emitter resistance and capacitance is low.

Accordingly, it is an object of the present invention is to provide an improved heterojunction bipolar transistor.

Another object of the present invention is to provide a heterojunction bipolar transistor having low emitter-base capacitance and low emitter resistance.

A further object of the present invention to provide a heterojunction bipolar transistor in which the bandgap differential between silicon and silicon-germanium is maintained.

SUMMARY OF THE INVENTION

The above and other objects and advantages of the present invention are achieved by a heterojunction bipolar transistor having a thin, lightly doped, silicon emitter disposed on a silicon-germanium base layer. The lightly doped silicon emitter maintains the bandgap differential between silicon-germanium and silicon. The silicon emitter is fabricated such that it will be depleted at zero bias so that emitter-base capacitance and emitter resistance is low. In one embodiment, a polysilicon contact layer may be formed on the silicon emitter and can be heavily doped to further reduce emitter resistance. In a second embodiment, a thin ohmic contact region may be formed in the silicon emitter instead of the polysilicon contact layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an enlarged, cross-sectional portion of a first embodiment of the present invention; and

FIG. 2 illustrates an enlarged, cross-sectional portion of a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates an enlarged, cross-sectional view of a portion of a heterojunction bipolar transistor in a first embodiment of the present invention. What is shown is a silicon layer 10 which acts as the collector of the heterojunction bipolar transistor, a silicon-germanium layer 12 which acts as the base, a thin silicon layer 14 formed on the silicon-germanium layer 12 which acts as the emitter, and a polysilicon layer 16 which acts as the emitter contact. A metal contact layer 18 is formed on polysilicon layer 16.

Silicon collector layer 10 is preferably doped N-type, using arsenic or antimony as a dopant. Silicon-germanium base layer 12 is preferably doped P-type, using boron as a dopant at approximately 1×10^{19} to 3×10^{19} atoms/cm^3. The thickness of silicon-germanium base layer 12 is preferably approximately 500 angstroms. Thin silicon layer 14 is preferably lightly doped N-type, using arsenic as a dopant at approximately 8×10^{16} to 3×10^{17} atoms/cm^3. The thickness of silicon layer 14 is preferably approximately 500 to 1500 angstroms. The thickness and doping of silicon layer 14 should be chosen such that silicon layer 14 will be substantially depleted at zero bias during normal operation. This is necessary in order to reduce emitter-base capacitance and emitter resistance. If silicon layer 14 is too thick, for example 4,000 angstroms as is described in the prior art, silicon layer 14 will not be depleted at zero bias and emitter resistance will be high. Polysilicon layer 16 is preferably heavily doped N-type using arsenic as a dopant.

After doping polysilicon layer 16, it is critical to anneal the heterojunction bipolar transistor by rapid thermal anneal to prevent degradation of the bandgap differential of silicon layer 14 and silicon-germanium layer 12 by preventing the diffusion of arsenic and boron from silicon-germanium layer 12 and silicon layer

14. Polysilicon layer 16 is heavily doped in order to further lower emitter resistance. In a preferred embodiment, polysilicon layer 16 is doped using arsenic as a dopant at a level of approximately greater than 1×10^{19} atoms/cm^3. The above layers are formed using techniques well known in the art. Note that only the active region of a heterojunction bipolar transistor is shown and described, however, this structure may be readily incorporated into many heterojunction bipolar process.

By including silicon layer 14 the metallurgical junction will be at the interface between silicon layer 14 and silicon-germanium layer 12. Thus, the advantage of the bandgap differential is not lost as in the prior art. In addition, the heterojunction bipolar transistor of the present invention has low emitter resistance and low emitter-base capacitance. The low emitter resistance is obtained by forming a heavily doped polysilicon layer 16. The low emitter-base capacitance is obtained by designing silicon layer 14 to be substantially depleted during operation. The heterojunction bipolar transistor of the present invention is thus a very high speed device that can be used for high speed digital and microwave applications.

FIG. 2 illustrates an enlarged, cross-sectional view of a portion of a heterojunction bipolar transistor in a second embodiment of the present invention. The same elements shown in FIG. 1 are referenced by the same numerals. FIG. 2 illustrates a structure similar to that of FIG. 1, however, in FIG. 2 polysilicon layer 16 is not utilized. In addition, silicon layer 14 is preferably slightly thicker than in FIG. 1. Silicon layer 14 is preferably approximately 1,000 to 2,500 angstroms so that a shallow emitter contact region 17 may be formed therein. Emitter contact region 17 is preferably formed by using a heavy dose of arsenic, and is just deep enough to provide ohmic contact to metal layer 18. In this second embodiment, as in the first embodiment, silicon emitter layer 14 is thin enough so that it is substantially depleted during operation. Thus, the structure of FIG. 2 also exhibits good electrical properties.

As can be readily seen, the heterojunction bipolar transistor of the present invention maintains the bandgap differential, thus exhibits high emitter injection efficiency, reduced charge storage in the emitter, reduced or eliminated hole injection into the emitter. In addition the heterojunction bipolar transistor of the present invention exhibits low emitter resistance and emitter-base capacitance by utilizing a thin silicon emitter layer.

We claim:

1. A heterojunction bipolar transistor, comprising:
- a collector;
- a silicon-germanium base disposed on the collector;
- a thin silicon emitter disposed on the silicon-germanium base, wherein a metallurgical junction is maintained at the silicon-germanium base and the thin silicon emitter interface; and
- a polysilicon layer disposed on the thin silicon emitter.

2. The heterojunction bipolar transistor of claim 1 wherein the silicon emitter is of a thickness where the thin silicon emitter is substantially depleted at zero bias.

3. The heterojunction bipolar transistor of claim 2 wherein the silicon emitter is of a thickness of approximately 500 to 2,500 angstroms.

4. A heterojunction bipolar transistor comprising:
- a collector;
- a silicon-germanium base formed on the collector;
- a thin silicon emitter formed on the silicon-germanium base, wherein the silicon emitter has a thickness and a doping level such that it is substantially depleted during normal operation, and wherein a metallurgical junction is maintained at the silicon-germanium base and the thin silicon emitter interface; and
- a polysilicon layer formed on the silicon layer.

5. The heterojunction bipolar transistor of claim 4 wherein the silicon emitter is of a thickness of approximately 500 to 2,500 angstroms.

6. The heterojunction bipolar transistor of claim 4 wherein the polysilicon layer is heavily doped.

7. A heterojunction bipolar transistor, comprising:
- an N-type collector;
- a P-type silicon-germanium base formed on the collector;
- an N-type, thin, lightly doped silicon emitter formed on the silicon-germanium base, wherein a metallurgical junction is maintained at the P-type silicon-germanium base and the N-type, thin, lightly doped silicon emitter interface; and
- an N-type, heavily doped polysilicon layer formed on the silicon layer.

8. The heterojunction bipolar transistor of claim 7 wherein the thin, lightly doped silicon emitter is substantially depleted during normal operation.

9. The heterojunction bipolar transistor of claim 8 wherein the thin, lightly doped silicon emitter is doped at approximately 8×10^{16} to 3×10^{17} atoms/cm^3.

10. The heterojunction bipolar transistor of claim 7 wherein the heavily doped polysilicon layer is doped at approximately 1×10^{19} atoms/cm^3.

* * * * *

Exhibit F

US005172214A

United States Patent [19]

Casto

[11] Patent Number: 5,172,214

[45] Date of Patent: Dec. 15, 1992

[54] **LEADLESS SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME**

[75] Inventor: **James J. Casto**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **866,282**

[22] Filed: **Apr. 10, 1992**

Related U.S. Application Data

[63] Continuation of Ser. No. 651,165, Feb. 6, 1991, abandoned.

[51] **Int. Cl.**[5] **H01L 23/28**; H01L 21/56

[52] **U.S. Cl.** **257/676**; 437/211; 437/220; 437/902; 257/693; 257/796; 257/737

[58] **Field of Search** 357/72, 68, 69, 70, 357/81; 437/211, 220, 902

[56] **References Cited**

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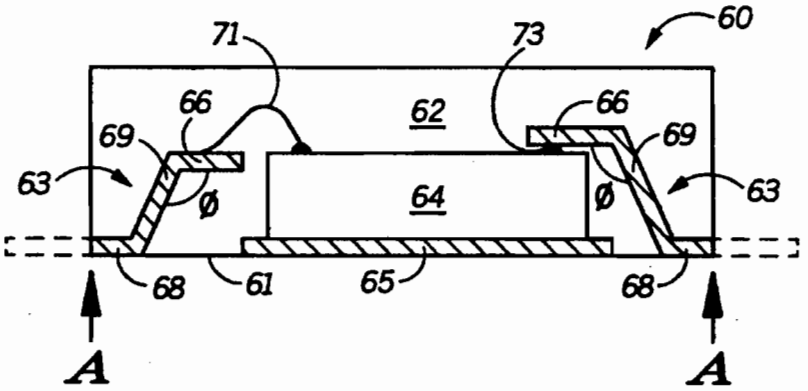
Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Patricia S. Goddard

[57] **ABSTRACT**

A semiconductor device having a thin package profile is leadless, thereby minimizing necessary mounting space on a substrate. In one form, a semiconductor device has a semiconductor die electrically coupled to a plurality of conductive leads. Each lead has a first portion, a second portion, and an intermediate portion which separates the first and second portions. A package body encapsulates the semiconductor die and the first and intermediate portions of the leads. The second portions of the leads are exposed on the bottom surface of the package body and are used to electrically access the semiconductor die.

12 Claims, 1 Drawing Sheet



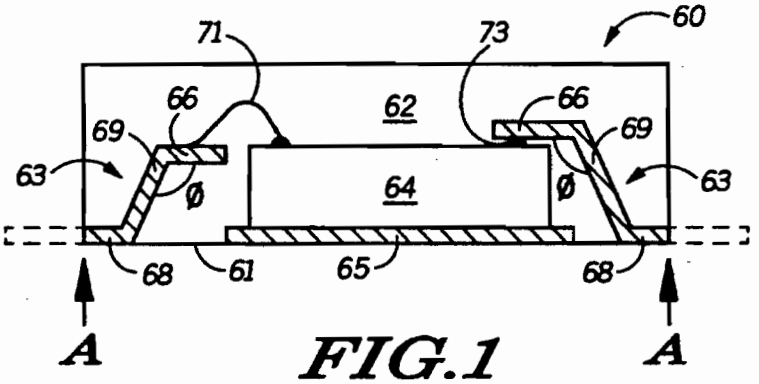


FIG.1

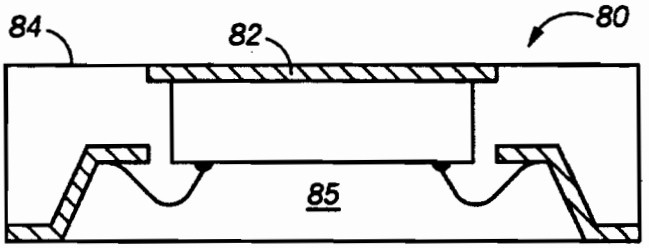


FIG.2

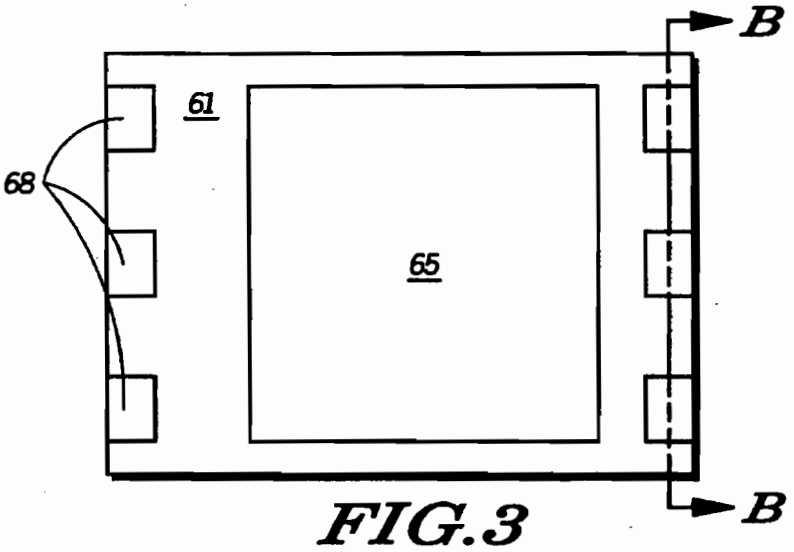


FIG.3

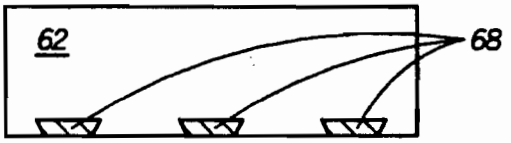


FIG.4

LEADLESS SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

This application is a continuation of prior application Ser. No. 07/651,165, filed Feb. 6, 1991, now abandoned.

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to a commonly assigned co-pending patent application entitled, "SEMICONDUCTOR DEVICE HAVING DUAL ELECTRICAL CONTACT SITES AND METHOD FOR MAKING THE SAME," by McShane et al., Ser. No. 07/651,166, filed concurrently herewith.

TECHNICAL FIELD OF THE INVENTION

The present invention is related to semiconductor devices in general, and more specifically, to leadless semiconductor devices having thin package profiles and a method for making the same.

BACKGROUND OF THE INVENTION

In order to meet the demands of the growing electronics industry, semiconductor manufacturers are faced with many challenges in supplying suitable semiconductor devices. One challenge is to provide customers with very small, yet powerful, devices. However, this challenge is not easily met. Small devices are desirable because small devices require less mounting space on a substrate and have fewer problems with signal transmissions as compared to larger devices. At the same time, powerful devices are necessary in order to store and transmit a maximum amount of imformation. Yet as the power and performance of a device increases, the size of the device also increases. Much of this increase is due to a larger number of terminals, or leads, required to operate the device.

Keeping the size of a semiconductor device to a minimum is often achieved by using thin, fragile, densely spaced leads as electrical contacts to the device. However, the use of such leads creates a variety of manufacturing and handling problems. Handling devices with such fragile leads can result in bent and non-coplanar leads, making it difficult to properly mount the device to a substrate, such as a PC (printed circuit) board. Manufacturing devices with such closely spaced leads is itself difficult. Leadframes used in molded packages have a piece of metal, known as a dambar, to act as a dam for molding material. The dambar must be cut out from between the leads prior to using the device, usually by a punching operation. Closely spaced leads can be damaged by the punching operation. Furthermore, the small dimensions of a punching tool used for removing dambars from between fine leads make the punching tool susceptible to damage as well.

Although much of the effort devoted to reducing package size has concentrated on reducing the package width and length, it is also desirable for semiconductor devices to be thin, especially in consumer electronics applications. Therefore, a need exists for an improved semiconductor device, and more specifically for an improved semiconductor device which is leadless and has a thin package profile.

BRIEF SUMMARY OF THE INVENTION

The previously mentioned needs are fulfilled, and other advantages are achieved with the present invention. In one form, a semiconductor device has a semiconductor device die. The semiconductor device die is electrically coupled to a plurality of conductive leads. Each lead has a first portion and a second portion, the first portion being separated from the second portion by an intermediate portion. A package body encapsulates the semiconductor device die and first and intermediate portions of the plurality of conductive leads. The second portions of the plurality of conductive leads are exposed on an edge and a bottom surface of the package body.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 illustrates, in cross-section, an embodiment of a semiconductor device in accordance with the present invention.

FIG. 2 illustrates, in cross-section, another embodiment of a semiconductor device in accordance with the present invention.

FIG. 3 illustrates, in planar view, the bottom surface of the semiconductor device of FIG. 1.

FIG. 4 illustrates, in cross-section, a view of the semiconductor device of FIG. 3 taken along the line B—B.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention has several advantages over conventional semiconductor devices. One advantage is that a semiconductor device in accordance with the present invention is externally leadless. Most known devices have leads which are external to a package body. The presence of external leads requires that a device occupy more space on a substrate, such as a printed circuit board, than if the device had no external leads. Furthermore, the presence of leads generates handling and manufacturing problems as discussed earlier. Some known semiconductor devices are considered to be leadless, for example a leadless chip carrier (LCC). However, most LCCs are formed from a multilayer ceramic material, and therefore LCCs are quite expensive. An overmolded device is also leadless, but overmolded devices require a semiconductor die to be mounted onto a PC board prior to encapsulation. Since an overmolded device contains a portion of a PC board, the cost of the device is significantly increased.

Another advantage of the present invention is that a semiconductor device can be made very thin, up to half the thickness of many conventional devices. Thin semiconductor devices are a competitive advantage in the consumer market for such applications as smart cards, cellular telephones, and pagers. Yet another advantage is that the present invention also allows a semiconductor device to have good heat dissipation, without increasing the size of the device. Heat dissipation is an important concern in high performance and high power consumption devices. Most methods of removing heat from a device, such as using heat sinks, increase the size of the device. The present invention can effectively dissipate heat without an increase in device size.

Illustrated in FIG. 1 is a semiconductor device 60 in accordance with the present invention. Device 60 has a semiconductor device die 64 which is usually an integrated circuit. Also included in device 60 is a leadframe (not entirely shown) having a plurality of leads 63 and a die receiving area 65 also known as a die pad or flag. Conventional leadframe materials, such as copper, copper alloys, iron-nickel alloys, or TAB (tape automated bonding) leadframes, are suitable for use with the pres-

ent invention. Semiconductor device die 64 is positioned at die receiving area 65, typically using an adhesive material, and is electrically coupled to the plurality of leads 63. The left portion of device 60 illustrated in FIG. 1 uses a wire bond 71 to couple a lead to the die, whereas the right portion of device 60 illustrates use of a TAB bond 73 or other type of lead-on-chip bond. Usually a semiconductor device contains only one type of coupling technique. The device of FIG. 1 has two different coupling techniques solely for illustrative purposes.

Device 60 is approximately one-half the thickness of a conventional molded semiconductor device. Most semiconductor devices have a package body which extends both above and below a plurality of leads of a leadframe. The device illustrated in FIG. 1 is thinner than many known devices because a protective package body 62 is formed only above the plurality of leads 63 of the leadframe. This is accomplished by forming the package in a one-sided mold tool or a mold tool having one planar platen. Typically, molded semiconductor device packages are formed in mold tools having an upper and a lower platen, each platen having a cavity. The platens are brought together such that the two cavities form a larger cavity which surrounds a semiconductor device die and inner portions of leads of a leadframe. An encapsulating material is introduced into the larger cavity to form a package body which completely surrounds a die and inner portions of the leads. The package body extends both above and below the die and the leads. Device 60, on the other hand, has package body 62 only formed above the leads 63 and semiconductor device die 64.

In accordance with the present invention, the leads 63 of device 60 in FIG. 1 have first portions 66, second portions 68, and intermediate portions 69. Second portions 68 of leads 63 are exposed on a bottom surface 61 of package body 62 and on the sides of the package body. Upon forming package body 62 about semiconductor device die 64, leads 63 will extend from the package body, as illustrated by the dashed lines in FIG. 1. The leads may then be formed into standard lead configurations, such as gull-wing, J-lead, through-hole, or the like. Preferably, leads 63 are severed at points A to create a leadless semiconductor device. Electrical contact to the semiconductor device is made through the second portions exposed on bottom surface 61 of the package.

As illustrated in FIG. 1, first portions 66 of leads 63 are portions of the leads which are electrically coupled to semiconductor device die 64. In the case of wire bond coupling, it is advantageous to have the bonding surface of a lead in the same plane as the bonding surface of the die. Naturally for the TAB bond illustrated, one surface must lie just above the other. Lead-on chip bonding may also be used in accordance with the present invention. Intermediate portions 69 of the leads are portions of the leads which join first portions 66 and second portions 68. In order to have the second portions of the leads exposed on the bottom surface of the package, yet have first portions coupled to the die, intermediate portions are at an angle with respect to both the first and second portions. For example, intermediate portions 69 of FIG. 1 are at an angle ϕ from first portions 66. Suitable angles for use with the present invention are substantially in the range of 90°–150°, although other obtuse angles could be used.

FIG. 1 also illustrates that die receiving area 65 is exposed on the bottom surface 61 of package body 62. Having the die receiving area, also referred to as a flag, exposed on a surface of the package improves the thermal performance of the device. Heat is conducted from semiconductor device die 64 through die receiving area 65 to the ambient, thereby reducing the temperature of the device.

To further enhance thermal performance, a die receiving area could be exposed on the top surface of the package body. Because the bottom surface of the package is adjacent to a substrate, such as a PC board, heat dissipation can be improved by removing heat through the top surface of the package rather than through the bottom surface. A semiconductor device 80, illustrated in FIG. 2, in accordance with the present invention, has a die receiving area 82 exposed on a top surface 84 of a package body 85. Device 80 has a thin package profile similar to the device illustrated in FIG. 1, yet has the added benefit of allowing heat to dissipate from a top surface which will be more exposed to the ambient.

A semiconductor device in accordance with the present invention, such as device 60 of FIG. 1, can be mounted to a substrate, such as a printed circuit board, like other leadless devices. For example, a PC board is screen printed with a solder paste in a pattern which corresponds to the pattern of the exposed second portions of the leads. The device is then appropriately positioned on the PC board and the solder is reflowed. For more reliable board mounting, the exposed portions of the leads of the device can be pretinned or solder plated prior to mounting the device. This improves the wettability of the exposed portions of the leads and provides better coupling to the screen printed solder on the substrate. An alternative method of mounting a device in accordance with the present invention is with the use of solder balls. Solder balls could be attached to the exposed portions of the leads and then coupled to a substrate at a later point.

Illustrated in FIG. 3 is a bottom perspective of the semiconductor device illustrated in FIG. 1. Die receiving area 65 is exposed on bottom surface 61 of the package body. Also exposed on bottom surface 61 are second portions 68 of the leads. Second portions 68 are used to electrically access the semiconductor die (not shown) and are usually electrically coupled to a substrate, for example, by solder, solder balls, gold bumps, or the like. A cross-section of second portions 68 taken along the line B—B of FIG. 3 is illustrated in FIG. 4. The cross-sectional shape of second portions 68 is illustrated as being trapezoidal. While a trapezoidal shape is not an essential aspect of the present invention, it may be helpful to have a lead shape which secures or locks the leads into place in package body 62. Because more of the lead is exposed on the surface of the package than in conventional semiconductor devices, added features to keep leads in place may be necessary.

Thus it is apparent that there has been provided, in accordance with the invention, a leadless semiconductor device and a method for making the same that fully meets the advantages set forth previously. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, use of the invention is not limited to use in packages

having one semiconductor die, but may also be used with multiple component semiconductor devices. Nor is it necessary that a device in accordance with the invention have an exposed die receiving area. Furthermore, the invention is not limited to using the electrical coupling methods described or illustrated. Likewise, any method of mounting a semiconductor device having a structure in accordance with the invention is suitable. It is not intended that the invention be limited to the substrate mounting techniques described. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.

I claim:

1. A leadless semiconductor device comprising:

a leadframe having a die receiving area and a plurality of leads extending outwardly from positions adjacent the die receiving area, each of the leads having first and second portions and an intermediate portion, the first portion of each lead being closer to the die receiving area than the second portion, and each of the first and second portions being separated by the intermediate portion thereof;

a semiconductor die positioned at the die receiving area of the leadframe and electrically coupled to the plurality of leads; and

a package body having a top surface, a bottom surface, and a perimeter, wherein the semiconductor die, the plurality of leads, and the die receiving area are completely contained within the package body and wherein a first surface of each of the second portions of the leads and an entire surface of the die receiving area are exposed on and substantially flush with one of either the top surface or bottom surface of the package body.

2. The semiconductor device of claim 1 wherein a second surface of each of the second portions of the leads is exposed on and substantially flush with the perimeter of the package body and wherein only the first and second surfaces of the leads are exposed.

3. The semiconductor device of claim 1 further comprising means for electrically coupling the second portions of the leads exposed on the bottom surface of the package body to a substrate.

4. The semiconductor device of claim 3 wherein the means for electrically coupling the second portions of the leads to a substrate comprises solder.

5. A leadless semiconductor device comprising:

a semiconductor die;

a plurality of conductive leads electrically coupled to the semiconductor die, each lead having a first portion for electrical connection to the die and a second portion for subsequent electrical connection to the device, the second portion being separated from the first portion by an intermediate portion; and

a molded package body completely containing the semiconductor die and the plurality of conductive leads wherein a first surface of each second portion is exposed on, and substantially flush with, a side of the package body and a second surface of each second portion is exposed on, and substantially flush with one of either a top surface or a bottom surface of the package body and wherein only the first and second surfaces of the leads are exposed.

6. The semiconductor device of claim 5 further comprising a die receiving area for receiving the semiconductor die and wherein a surface of the die receiving area is exposed on and flush with one of either a top surface of the package body or the bottom surface of the package body.

7. The semiconductor device of claim 5 wherein the first portions of the leads and the second portions of the leads are positioned in substantially parallel planes.

8. The semiconductor device of claim 5 wherein the first portion of each of the plurality of leads intersects the intermediate portion at an obtuse angle.

9. A method for fabricating a leadless semiconductor device comprising the steps of:

providing a semiconductor die;

providing a leadframe having a die receiving area and a plurality of leads extending outwardly from positions adjacent the die receiving area, each of the leads having first and second portions and an intermediate portion, the first portion being closer to the die receiving area than the second portion, and the first and second portions being separated by the intermediate portion;

electrically coupling each first portion of the plurality of leads to the semiconductor die;

encapsulating the semiconductor die and portions of the plurality of leads with a resin encapsulating material to form a package body which completely contains the first portions, intermediate portions, and second portions of the leads such that a first surface of each of the second portions of the leads and an entire surface of the die receiving area are exposed on, and substantially flush with, one of either a top surface or a bottom surface of the package body; and

severing the plurality leads to create a second surface of each of the second portions of the leads which is exposed on, and substantially flush with, a side of the package to form the leadless semiconductor device in which only the first and second surfaces of the leads are exposed.

10. The method of claim 9 further comprising the step of attaching the semiconductor device to a substrate by soldering the exposed second portions of the leads on the bottom of the package body to the substrate.

11. A method for fabricating a leadless semiconductor device comprising the steps of:

providing a semiconductor die;

providing a leadframe having a plurality of leads, each of the leads having first and second portions and an intermediate portion, the first portions of the leads being used for electrical connection to the die, the second portions of the leads being used for electrical connection to the device, and the first and second portions being separated by the intermediate portion;

electrically coupling the first portions of each of the plurality of leads to the semiconductor die;

forming a package body from a resin encapsulating material, the package body completely containing the semiconductor die and the first, second, and intermediate portions of the plurality of leads such that a first surface of each of the second portions of the leads is exposed on, and substantially flush with, either a top surface or a bottom surface of the package body, such that a second surface of each second portion of the leads is exposed on, and substantially flush with a side of the package body, and such that only the first and second surfaces of the leads are exposed; and

plating the first and second exposed surfaces of the second portions of the leads with a conductive material.

12. The method of claim 11 wherein the step of plating the exposed areas of the second portions of the leads with a conductive material comprises plating the exposed areas of the second portions of the leads with solder.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,172,214

DATED : December 15, 1992

INVENTOR(S) : James J. Casto

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In claim 1, column 5, line 36:
after "package body" insert --wherein a second surface of each of the second portions of the leads is exposed on and substantially flush with the perimeter of the package body, and wherein only the first and second surfaces of the second portions of the leads are exposed--;

Cancel claim 2;

In claim 5, column 5, line 65:
after "second surfaces" insert --of the second portions--;

In claim 9, column 6, line 38:
after "second surfaces" insert --of the second portions--; and

In claim 11, column 6, line 67:
after "second surfaces" insert --of the second portions--.

On title page, "12 Claims, 1 Drawing Sheet" should read

--11 Claims, 1 Drawing Sheet--

Signed and Sealed this

Sixteenth Day of November, 1993

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

[redacted]

Exhibit G

US005195655A

United States Patent [19]

Bukhman

[11] **Patent Number: 5,195,655**

[45] **Date of Patent: Mar. 23, 1993**

[54] **INTEGRATED FLUID DISPENSE APPARATUS TO REDUCE CONTAMINATION**

[75] Inventor: **Yefim Bukhman**, Scottsdale, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **705,197**

[22] Filed: **May 24, 1991**

[51] **Int. Cl.**[5] **B65D 35/28**

[52] **U.S. Cl.** **222/1**; 222/95; 222/571; 239/589

[58] **Field of Search** 222/4, 64, 95, 105, 222/107, 131, 145, 146.5, 146.2, 148, 187, 403, 423, 541, 571, 575, 568; 239/128, 135, 589, 601, 44

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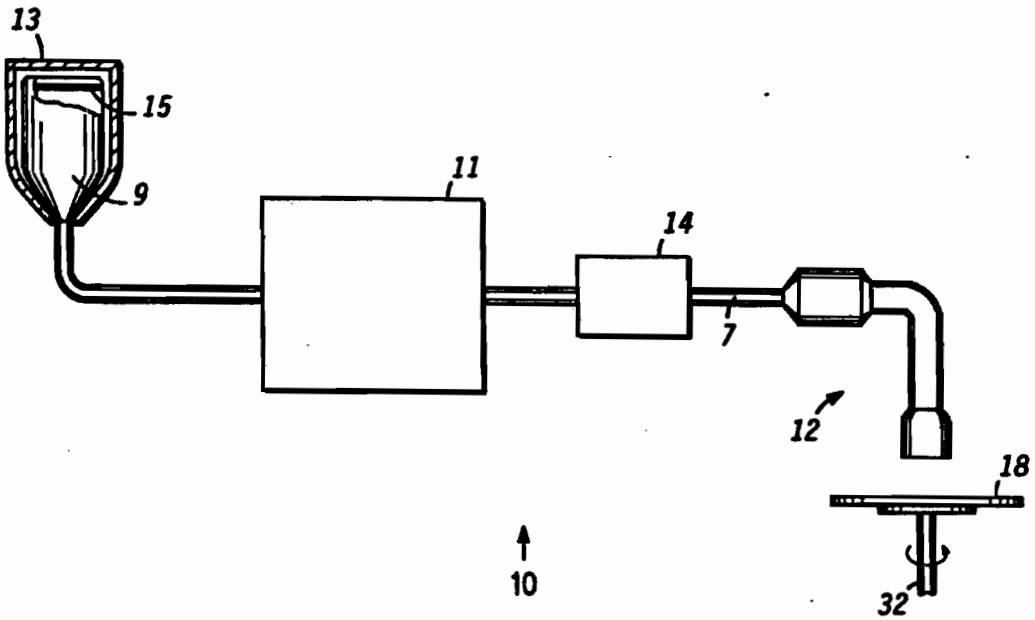
Assistant Examiner—Kenneth DeRosa
Attorney, Agent, or Firm—Joe E. Barbee

[57] **ABSTRACT**

An integrated fluid dispense apparatus (10) suitable for delivering ultrapure fluids. The fluid is confined to a nonrigid hermetic fluid delivery apparatus (10). A pumping mechanism (11) pumps fluids in precise volumes and flow rates. A moisturizing dispense nozzle (12) provides a saturated vapor atmosphere at the nozzle tip to prevent the fluid from drying during non-dispense periods.

16 Claims, 2 Drawing Sheets



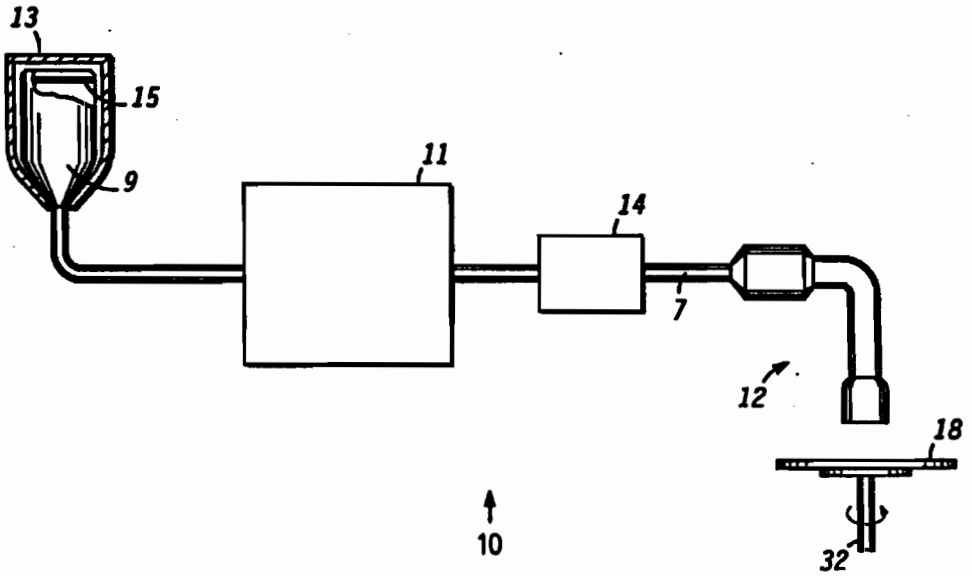
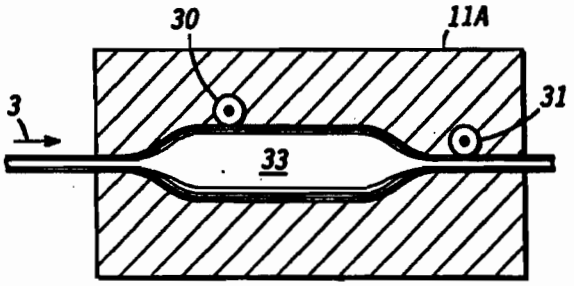


FIG. 1

FIG. 2



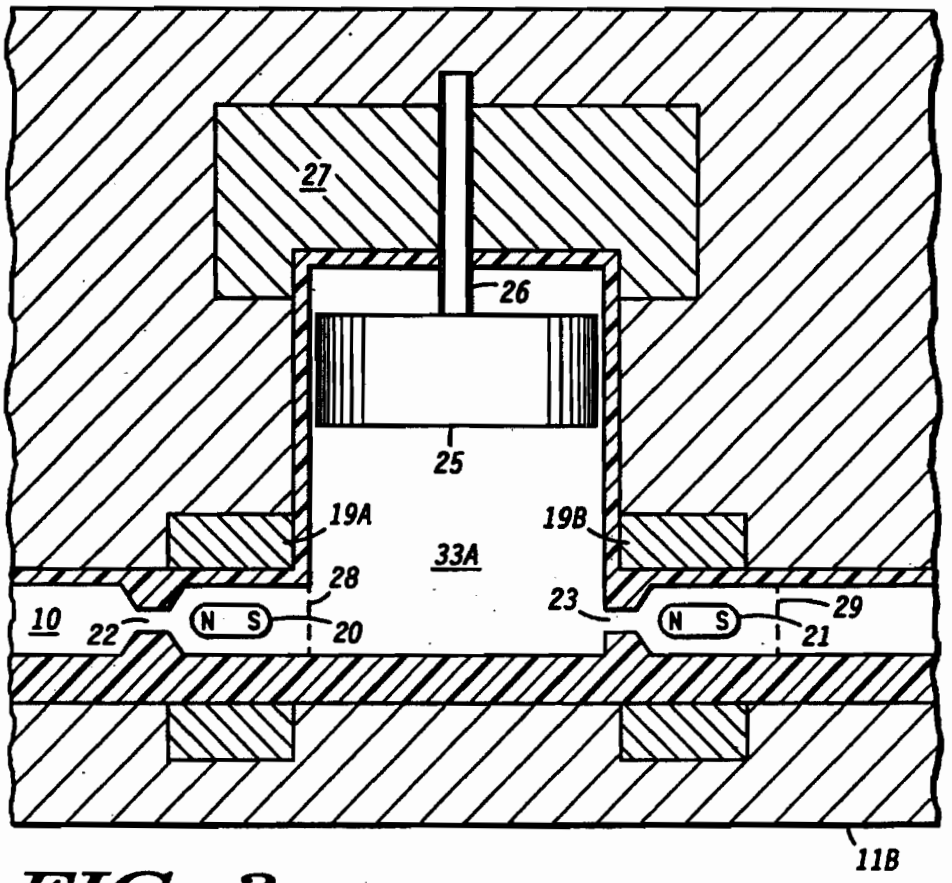

27
26
25
19A
19B
33A
28
23
29
10
22
N S
20
N S
21
11B

FIG. 3

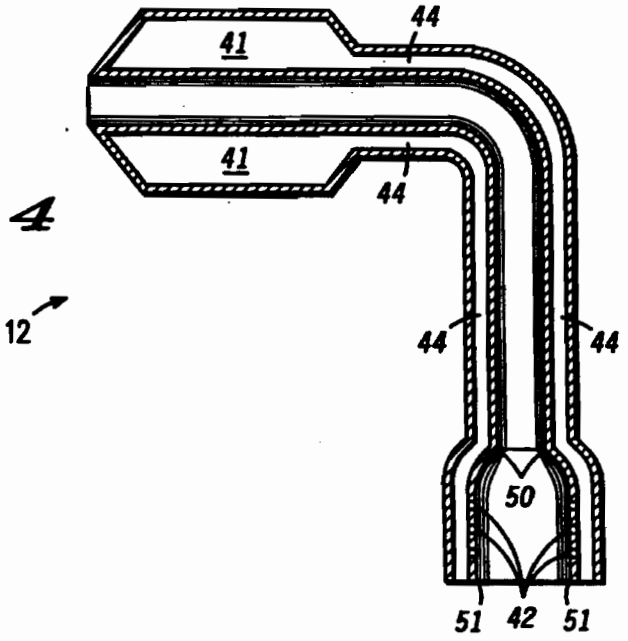

44
41
41
44
12
44
44
50
51
42
51

FIG. 4

INTEGRATED FLUID DISPENSE APPARATUS TO REDUCE CONTAMINATION

BACKGROUND OF THE INVENTION

This invention relates, in general to fluid delivery systems, and more particularly to an ultrapure fluid delivery system.

Fluid delivery systems are found in a variety of industries including electronics, medical, food, and beverage. Generally, these systems have employed replaceable glass bottle fluid reservoirs and pumping mechanisms to deliver the fluid from the reservoir to a nozzle. Inherent in these fluid transport regimes is the introduction of contaminants during fluid reservoir replacement. As an example, reservoir replacement entails disconnecting the fluid delivery lines, thereby opening the fluid delivery system to contamination by particulates and air bubbles. Further, the pumping mechanism and fluids themselves are sources of particulates, hence filters may be included in the system. Changing the filters, pumps or any component in the system serves as a means for contaminant entry into the system. In addition, the construction of the nozzles through which the fluid is dispensed promotes the drying and subsequent flaking of the fluid; in a photoresist delivery system these flakes would contaminate the photoresist deposited on a wafer. Accordingly, it would be beneficial to have a fluid delivery system, such as a photoresist dispenser for use in manufacturing semiconductor products, that does not introduce contaminants into the fluid being delivered.

SUMMARY OF THE INVENTION

Briefly stated, the present invention has an integrated fluid dispense apparatus consisting of a nonrigid hermetic fluid delivery apparatus, a moisturizing dispense nozzle, and a means for pumping fluid through the hermetic fluid delivery apparatus to the moisturizing dispense nozzle. The nonrigid hermetic fluid delivery apparatus has a portion adapted to cooperate with the means for pumping and a portion that serves as a fluid reservoir.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cut-away side view of an embodiment in accordance with the present invention;

FIG. 2 is a cut-away side view of an embodiment of a fluid pumping mechanism;

FIG. 3 is a cut-away side view of an alternate embodiment of a fluid pumping mechanism; and

FIG. 4 is a cut-away side view of an embodiment of the solvent delivering moisturizing nozzle.

DETAILED DESCRIPTION OF THE DRAWINGS

A cut-away side view of an integrated fluid dispense apparatus **10** is illustrated in FIG. 1. Integrated fluid dispense apparatus **10** is a nonrigid structure. Nonrigid fluid delivery apparatus **10** is a disposable hermetic unitary unit coupled to a moisturizing dispense nozzle **12**. Nonrigid fluid delivery apparatus **10** has a collapsible fluid reservoir **9** supported by a housing **13**. In a preferred embodiment, housing **13** also includes a level sensing means (not shown). In an alternate embodiment, housing **13** also includes a means **15** for promoting uniform collapse of collapsible fluid reservoir **9**. A portion of nonrigid fluid delivery apparatus **10** is adapted to contain specified fluid volumes and to cooperate with a pumping mechanism **11** for pumping fluid towards moisturizing dispense nozzle **12**. Pumping mechanism **11** pumps a predetermined fluid volume at a specified flow rate. Pumping mechanism **11** also creates a reverse pressure or suction, commonly called suckback, during nonpumping cycles to prevent fluid dispensation.

In a preferred embodiment, a portion of nonrigid fluid delivery apparatus **10** is surrounded by or in contact with a heater **14** for regulating the temperature of the fluid. Heater **14**, which is thermostatically controlled, serves as a means for regulating fluid temperature. In an optional embodiment, nonrigid fluid delivery apparatus **10** includes a filter **7**. Filter **7** removes any impurities not removed by the fluid manufacturer. Filter **7** is coupled to a portion of nonrigid fluid delivery apparatus **10** distal to collapsible fluid reservoir **9**.

Moisturizing dispense nozzle **12** generates a saturated vapor atmosphere. Nozzle **12** is a dry-less dispense nozzle. Nozzle **12** will be discussed in greater detail in the description of FIG. **4**. In a preferred embodiment, a cap (not shown) is used to seal or close the porous tip of moisturizing dispense nozzle **12** when moisturizing dispense nozzle **12** is in transit or not in use. The cap is a T-shaped element having a vertical segment or leg and a horizontal segment or head. The leg is inserted into the fluid dispensing tip of moisturizing dispense nozzle **12**, and is held in position by a friction fit. The head is larger than the opening of moisturizing dispense nozzle **12** and prevents any contaminants from entering the moisturizing dispense nozzle **12**.

Moisturizing dispense nozzle **12** dispenses a photoresist onto a semiconductor wafer **18** while semiconductor wafer **18** is being rotated by a shaft **32**. Since a specific amount of photoresist is to be applied to wafer **18**, pumping mechanism **11** forces only the specified amount of photoresist out of the moisturizing dispense nozzle **12**. To prevent any excess drops from falling onto wafer **18**, pump **11** has the capability of creating a reverse pressure or suckback to draw any photoresist at the tip of nozzle **12** back up into nozzle **12**.

FIG. **2** is a cut-away side view of pumping mechanism **11A**; including a portion of nonrigid fluid delivery apparatus **10** (shown in FIG. **1**) adapted to cooperate with pumping mechanism IIA called a pumping pouch **33**. Pumping mechanism IIA has a pumping roller **30** and a suckback roller **31**. Pumping roller **30** and suckback roller **31** move up, down, and to the right and left. Pumping roller **30** has a home position which is above, but not in contact with pumping pouch **33**, and proximal to the pump inlet. Suckback roller **31** has a home position which is above, but not in contact with pumping pouch **33**, and distal to the pump inlet. Suckback roller **31** functions as a valve; the valve is defined as open when suckback roller **31** is in the home position.

To pump fluid, pumping roller **30** moves down from its home position and seals a portion of pumping pouch **33** proximal to pump inlet. After pumping roller **30** seals pumping pouch **33**, suckback roller **31** moves to the suckback roller **31** home position and pumping roller **30** moves to the right. The rate at which pumping roller **30** moves to the right modulates the fluid dispense rate. After pumping the specified fluid volume, suckback roller **31** terminates active fluid flow by moving down from the suckback roller **31** home position and sealing a portion of pumping pouch **33** distal to the pump inlet. Suckback roller **31** creates reverse pressure or suckback by moving to the left. Pumping roller **30** moves to

pumping roller 30 home position to be in position for the start of the next pumping cycle. In a preferred embodiment, positioning of pumping roller 30 and suckback roller 31 is computer controlled; where pumping roller positioning serves as a means for controlling fluid volume and suckback roller positioning serves as a means for controlling the reverse pressure or suckback. The arrow 3 indicates direction of fluid flow.

FIG. 3 is a cut-away side view of an alternate embodiment of a portion of nonrigid fluid delivery apparatus 10 which cooperates with a pumping mechanism IIB to pump fluid. Pumping mechanism IIB comprises a plunger 25, a pushrod 26, and an actuator 27. The portion of nonrigid fluid delivery apparatus 10 adapted to cooperate with pumping mechanism IIB is a pumping pouch 33A also referred to as a pumping container. Pumping pouch 33A has an inlet port which comprises an inlet port channel 22, an inlet port magnetic valve 20, and an inlet port perforated stop 28. Pumping pouch 33A has an outlet port which comprises an outlet port channel 23, an outlet port magnetic valve 21, and an outlet port perforated stop 29. In a preferred embodiment, the nonrigid fluid delivery apparatus 10 is a unitary unit; however, in an alternate embodiment, the pumping pouch 33A is a disposable detachable unit which may be mated with hoses at the inlet and outlet ports. Inlet magnetic valve 20 and outlet magnetic valve 21 are controlled by electromagnets 19A and 19B, respectively.

To pump fluid, electromagnet 19A closes inlet magnetic valve 20. After inlet magnetic valve 20 seals inlet port 22, electromagnet 19B opens outlet magnetic valve 21. Actuator 27 actuates pushrod 26 to distend plunger 25, forcing fluid to flow toward moisturizing dispense nozzle 12. After pumping the specified fluid volume, actuator 27 actuates pushrod 26 to contract plunger 25, creating reverse pressure or suckback. Electromagnet 19B closes outlet magnetic valve 21. After outlet magnetic valve 21 seals outlet port 23, electromagnet 19A opens inlet magnetic valve 20 to begin the next pumping cycle. In a preferred embodiment, electromagnets 19A, 19B, and actuator 27 are computer controlled.

FIG. 4 is a cut-away side view of moisturizing dispense nozzle 12. A portion 41 of moisturizing dispense nozzle 12 is a solvent filled reservoir which is packed with a wicking material. A channel 44 extends from solvent reservoir 41 to a plurality of porous openings 42 at the tip of moisturizing dispense nozzle 12. Porous openings 42 deliver solvent as a saturated vapor atmosphere to the tip of moisturizing dispense nozzle 12 to keep the fluid or photoresist at the tip from drying out and forming a "skin"; resulting in flakes. The flakes would contaminate the photoresist deposited on wafer 18 (FIG. 1). The channel is filled with wicking material to facilitate movement of solvent by capillary action. Small quantities of solvent in saturated vapor form may mix with the fluid being dispensed; however, the volumes would be so minute as to have no affect on the volume, purity or dispense rate of the fluid being dispensed.

In a preferred embodiment, nonrigid fluid delivery apparatus 10 is a unitary unit; however, in an alternate embodiment the nozzle 12 can be separate from nonrigid fluid delivery apparatus 10, but adapted to fit over the tip of nonrigid fluid delivery apparatus 10. Tip of nonrigid fluid delivery apparatus 10 protrudes past the inner lip 50 of moisturizing dispense nozzle 12 but not past the outer lip 51 of moisturizing dispense nozzle 12.

By now it should be appreciated that there has been provided an improved fluid dispense apparatus suitable for delivering precise fluid volumes at precise dispense rates without the level of contaminants inherent in present fluid delivery systems. This apparatus is suitable for dispensing predetermined volumes of photoresist on a semiconductor wafer.

I claim:

1. A method for reducing fluid contamination comprising:
providing a reservoir for containing fluid;
providing means for cooperating with a pumping mechanism to pump the fluid; and
generating a saturated vapor atmosphere at a nozzle from which the fluid is dispensed to prevent the fluid from drying on the nozzle.

2. The method for reducing fluid contamination of claim 1 using a solvent as the saturated vapor atmosphere.

3. The method for reducing fluid contamination of claim 1 generating a slight back pressure at completion of a dispense operation to prevent dripping fluid from the nozzle.

4. The method for reducing fluid contamination of claim 1 wherein providing the reservoir includes providing a disposable reservoir.

5. An integrated fluid dispense apparatus comprising a fluid delivering dispense nozzle having means for moisturizing a tip of said nozzle to prevent the fluid from drying in the dispense nozzle; and a fluid delivery apparatus coupled to the dispense nozzle.

6. The integrated fluid dispense apparatus of claim 5 wherein the moisturizing means includes means for delivering a solvent to said tip of the dispense nozzle.

7. The integrated fluid dispense apparatus of claim 6 wherein the means for delivering the solvent includes a reservoir packed with wicking material.

8. The integrated fluid dispense apparatus of claim 6 wherein the means for delivering the solvent creates a saturated vapor atmosphere at the dispense nozzle tip, and wherein the fluid delivery apparatus ia nonrigid hermetic unitary unit.

9. An integrated fluid dispense apparatus to reduce contamination of the fluid by particles which comprises:
a nonrigid hermetic fluid delivery apparatus;
a housing to support a portion of the nonrigid hermetic fluid delivery apparatus that serves as a fluid reservoir;
a nozzle for dispensing the fluid and having means for moisturizing a tip of said nozzle to prevent the fluid from drying in the nozzle, wherein the nozzle is connected to the portion of the nonrigid hermetic fluid delivery apparatus distal to the fluid reservoir;
means for pumping the fluid through the nonrigid hermetic fluid delivery apparatus toward the nozzle, wherein the nonrigid hermetic fluid delivery apparatus has a portion adapted to cooperate with the means for pumping; and
means to regulate the temperature of the fluid prior to fluid dispensation.

10. The integrated fluid dispense apparatus of claim 9 wherein the nonrigid hermetic fluid delivery apparatus is a unitary unit.

11. The integrated fluid dispense apparatus of claim 9 wherein the nozzle and the nonrigid hermetic fluid delivery apparatus are a unitary assembly.

12. The integrated fluid dispense apparatus of claim 9 wherein the means for pumping includes means to prevent fluid dispensation during nonpumping cycles.

13. A photoresist delivery system to reduce contamination of the photoresist by particles which comprises:

a photoresist reservoir;

a pumping means wherein the pumping means is coupled to the photoresist reservoir; and

a dispense nozzle having means for moisturizing a tip of said nozzle to prevent the fluid from drying in the dispense nozzle wherein the dispense nozzle is coupled to the pumping means.

14. The photoresist delivery system of claim 13 wherein the photoresist reservoir is hermetically coupled to the dispense nozzle.

15. The photoresist delivery system of claim 13 wherein the pumping means includes means to prevent photoresist dispensation during nonpumping cycles.

16. The photoresist delivery system of claim 13 further including a housing to support the photoresist reservoir.

* * * * *

Exhibit H

US005200362A

United States Patent [19]

Lin et al.

[11] Patent Number: 5,200,362

[45] Date of Patent: Apr. 6, 1993

[54] METHOD OF ATTACHING CONDUCTIVE TRACES TO AN ENCAPSULATED SEMICONDUCTOR DIE USING A REMOVABLE TRANSFER FILM

[75] Inventors: Paul T. Lin; Michael B. McShane, both of Austin, Tex.; Sugio Uchida; Takehi Sato, both of Nagano, Japan

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 756,952

[22] Filed: Sep. 9, 1991

Related U.S. Application Data

[63] Continuation of Ser. No. 576,255, Aug. 31, 1990, abandoned.

[30] Foreign Application Priority Data

Sep. 6, 1989 [JP] Japan 1-231323

[51] Int. Cl.[5] H01L 21/56; H01L 21/58; H01L 21/60

[52] U.S. Cl. 437/207; 437/211

[58] Field of Search 437/206, 211, 220, 207; 264/272.17; 29/841, 855

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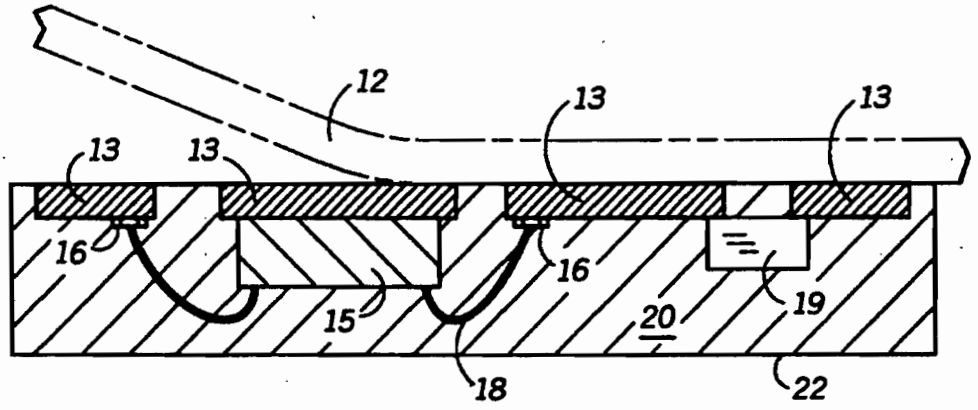
Primary Examiner—Olik Chaudhuri
Assistant Examiner—David E. Graybill
Attorney, Agent, or Firm—Jasper W. Dockrey

[57] ABSTRACT

A semiconductor device and a method for its fabrication are disclosed. In a preferred embodiment, a pattern of conductive traces is formed on a film of transfer material. A semiconductor device die is interconnected to the pattern of conductive traces and a resin body is formed around the die, one side of the conductive traces, and the interconnecting means. The film of transfer material forms, at this stage of the process, one side of the package. The film of transfer material is then peeled from the pattern of conductive traces and the resin body to expose the other side of the pattern of conductive traces. Contact to the other side of the pattern provides electrical contact to the semiconductor device die.

8 Claims, 3 Drawing Sheets



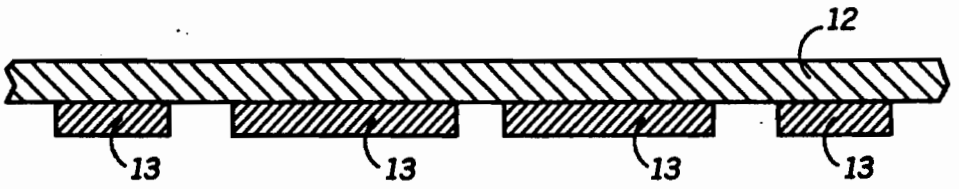


FIG.1

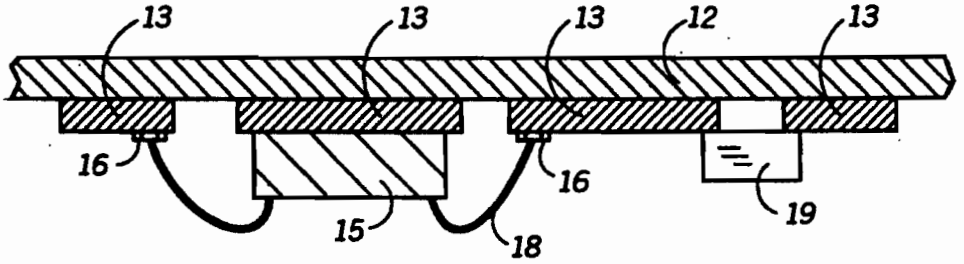


FIG.2

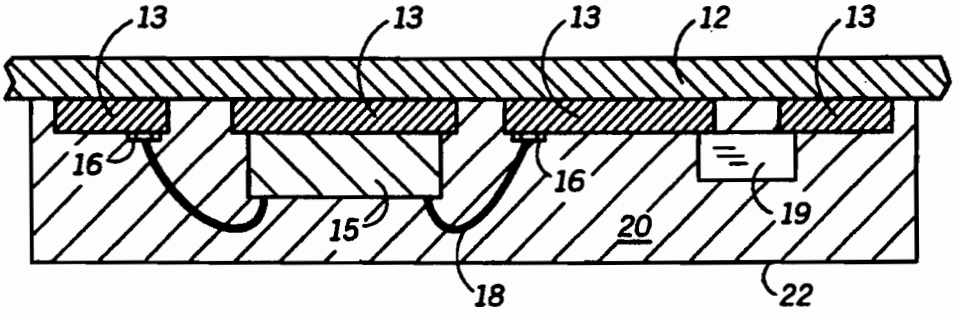


FIG.3

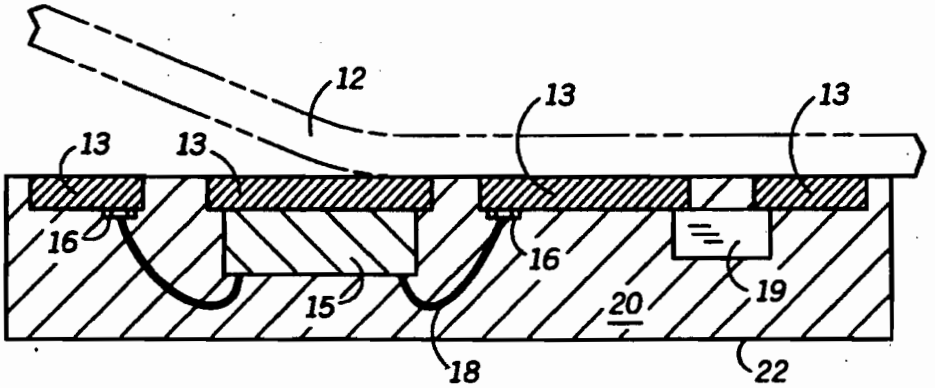


FIG.4

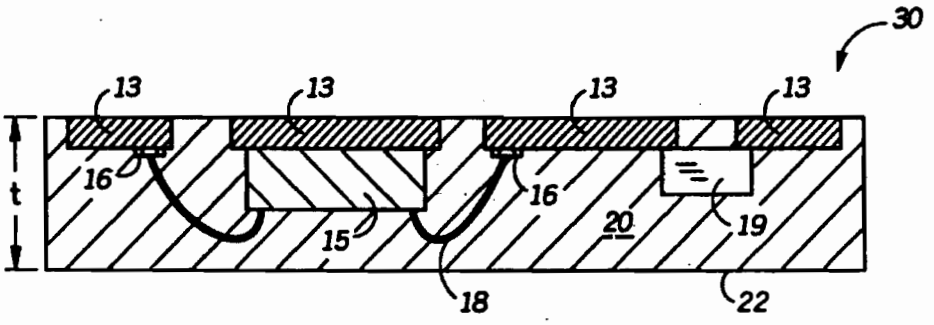


FIG.5

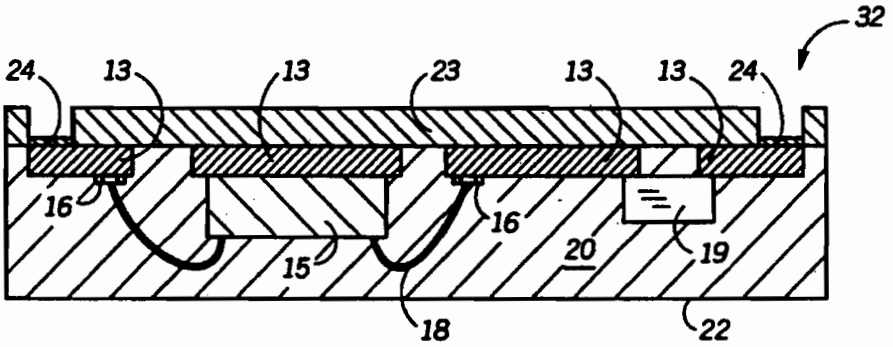


FIG.6

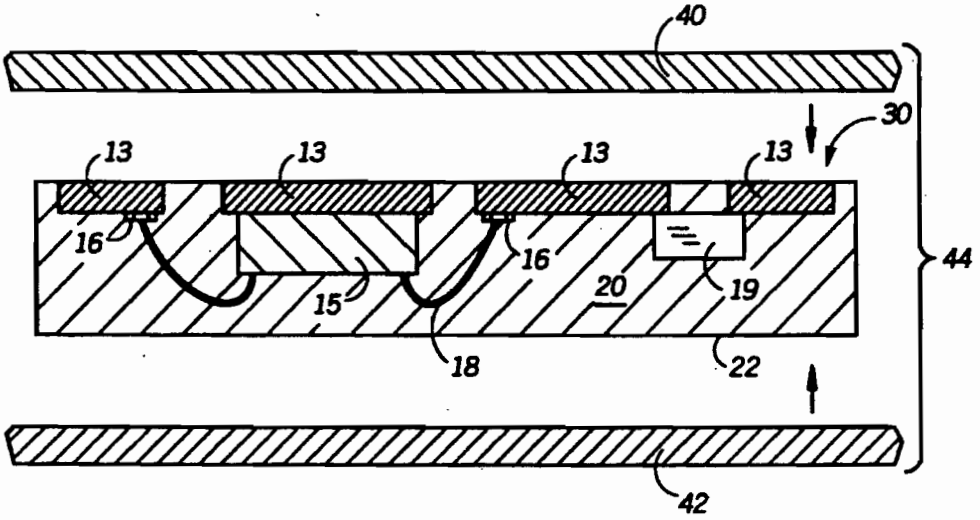


FIG.7

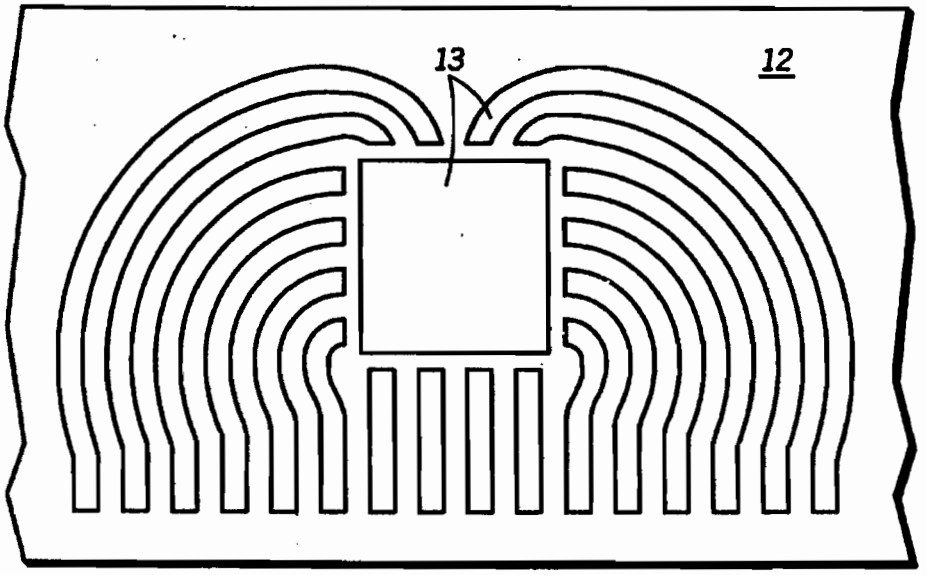


FIG.8

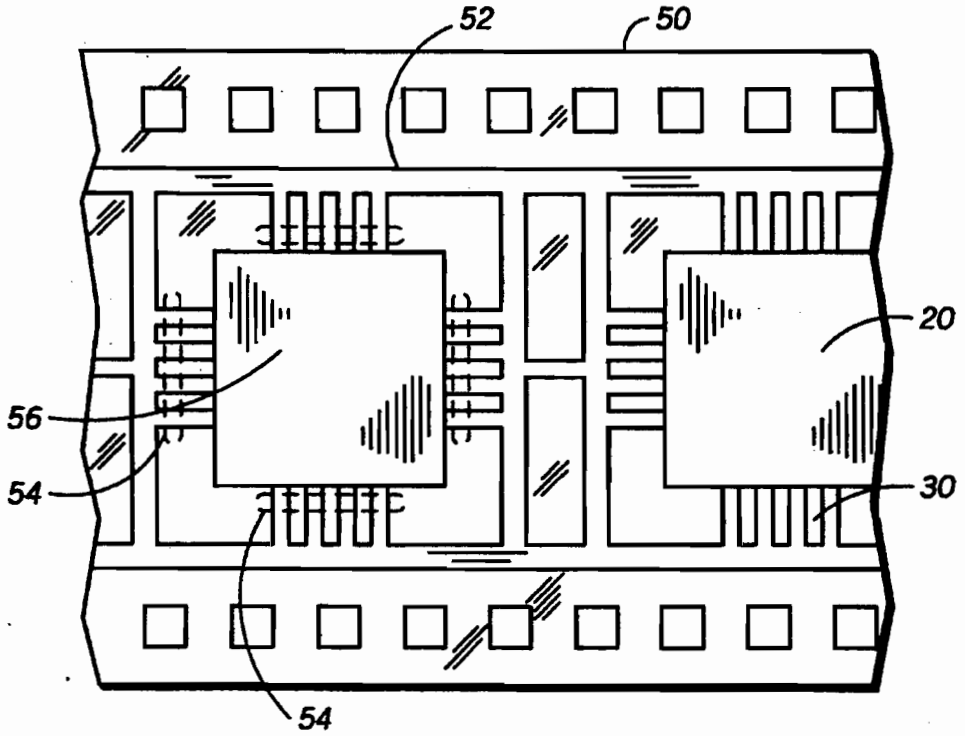


FIG.9

METHOD OF ATTACHING CONDUCTIVE TRACES TO AN ENCAPSULATED SEMICONDUCTOR DIE USING A REMOVABLE TRANSFER FILM

This is a continuation of application Ser. No. 07/576,255, filed Aug. 31, 1990, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a resin encapsulated semiconductor device and to a method for its fabrication, and more specifically to a resin encapsulated semiconductor device capable of being fabricated in a thin format.

Semiconductor devices are widely used in various types of electronic products, consumer products, automobiles, integrated circuit cards, and the like. One feature of the semiconductor device which is important in many of these applications, and especially in such applications as the integrated circuit card, is the small size of the semiconductor device.

The semiconductor devices which are used in those various applications are usually packaged by either one of two methods. In one method, a semiconductor device die is placed in a package which is then individually mounted on a circuit substrate. In an alternate method, the semiconductor device die itself is mounted directly on the circuit substrate and then is usually provided with a protective encapsulation structure. The first mentioned method has the advantages that the device die is sealed in and protected by the package. The packaged device is easy to test, handle, and install and the encapsulating package provides the desired degree of protection against the environment. In contrast, the second described method in which the device die is connected directly to the substrate minimizes the area required by the die and thus allows a very high packing density. In this method, however, the device die is less easily handled and tested and is more subject to undesirable effects of the environment.

In selecting either of the above mentioned packaging techniques, it is necessary to compromise in the characteristics of the semiconductor device and the way it is utilized. In addition, either method requires that the semiconductor device be packaged on the interconnecting substrate such as a PC board, and thus has a problem of preventing the reduction in the thickness of the substrate so that the semiconductor device cannot be used in an application such as an IC card which requires an extremely thin substrate.

Thus a semiconductor device and a method for its fabrication were needed which would overcome the limitations of the foregoing semiconductor devices and methods.

BRIEF SUMMARY OF THE INVENTION

This invention provides a highly reliable packaged semiconductor device and a method for its fabrication which achieves a reduction in the thickness of the device without compromising the ease of handling a fully packaged device. In accordance with one embodiment of the invention, a semiconductor device is fabricated by providing a transfer film on which a pattern of conductive traces are provided. A semiconductor device die is interconnected to the pattern of conductive traces and a resin material is provided to encapsulate the semiconductor device die, one side of the pattern of conductive traces, and the electrical interconnections between the traces and the die. The transfer film is then peeled from the encapsulated device and the pattern of conductive traces to expose the underside of the pattern of traces, at least a portion of which is available for making electrical contact to the semiconductor device die.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1–4 illustrate, in cross section, process steps in accordance with one embodiment of the invention for the fabrication of a semiconductor device;

FIGS. 5 and 6 illustrate, in cross section, semiconductor devices in accordance with two embodiments of the invention;

FIG. 7 illustrates schematically the fabrication of an integrated circuit (IC) card;

FIG. 8 illustrates a representative pattern of conductive traces on a transfer film; and FIG. 9 illustrates the fabrication of a plurality of semiconductor devices on an elongated transfer film in accordance with a further embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIGS. 1–4 illustrate, in cross section, process steps in accordance with one embodiment of the invention. As illustrated in FIG. 1, a transfer film 12 is provided with a pattern of conductive traces 13 on one side of the film. A representative and illustrative pattern of such traces is shown in FIG. 8. Transfer film 12 is a sheet film of flexible material such as "Kapton" or polyester upon which the pattern of conductive traces is formed.

The pattern of conductive traces can be formed in a number of differeht ways. In accordance with a preferred embodiment of the invention, a foil of conductive material such as copper is laminated to the transfer film 12 and is subsequently patterned using conventional photolithographic patterning and etching. Alternatively, the pattern of conductive traces can be formed, for example, by evaporating a layer of metal or other conductor onto the surface of the transfer film and then patterning that evaporated layer. If the evaporated layer is not of sufficient thickness to reduce the series resistance to a low enough value, the thickness can be increased by plating additional material onto the evaporated film. Still further, the pattern of conductive traces can be formed by first applying a reverse photoresist mask to the transfer film, evaporating a conductive material onto the photoresist and the transfer film, and then using a lift off process to remove the unwanted conductive material. In yet another embodiment, a pattern of traces is formed from a thin sheet of metal and that pattern of traces is then laminated to the transfer film.

A semiconductor device die 15 is electrically interconnected to the pattern of conductive traces. The interconnection is accomplished by wirebonds 18 or by other conventional means such as TAB tape, or the like. The semiconductor die can be affixed to a portion of the pattern of conductive traces, for example by solder, conductive epoxy, or the like or can be attached to the pattern only by the interconnecting means 18. If the die is attached to a portion of the pattern of conductive traces, that portion can be used, if necessary, as an electrical contact to a substrate of the semiconductor device die. As also illustrated in FIG. 2, additional circuit elements 19 can also be attached to and interconnected with the pattern of conductive traces. Circuit element

19 can be, for example, a resistor, diode, capacitor, or the like. The additional circuit element, which can also be an additional semiconductor device die, can be connected between traces, as illustrated, or can be bonded to the conductive traces as is device die 15.

The portion 16 of the pattern of conductive traces to which the wirebonds or other interconnecting means are joined can be prepared especially to accommodate the attachment of the interconnecting means. For example, the bonding area 16 can be plated with gold, treated to smooth the area, or otherwise treated to enhance the reliability of the interconnection.

As illustrated in FIG. 3, the process continues by the encapsulation of the semiconductor device die 15, additional circuit element 19, interconnecting means 18, and one side of the pattern of conductive traces by an encapsulating resin 20 to form a protective body 22. Body 22 is formed in conventional manner, such as by transfer molding in which the transfer film 12 with the attached semiconductor device die 15 is inserted into a mold cavity and the encapsulating resin is forced into the cavity at a high temperature and high pressure. Alternatively, body 22 can be made by injection molding, pour molding, or in a "glop top" process. In each of these encapsulating operations, the resin material is formed on one side of transfer film 12; that is, the transfer film, at this stage of the process, forms one side of the package. The resin material thus surrounds the semiconductor device die, the interconnecting means, and one side of the pattern of conductive traces, plus any additional electronic components which are attached to the conductive traces.

Following the encapsulation operation, as illustrated in FIG. 4, the transfer film 12 is peeled or removed from the surface of the encapsulated device leaving a resin encapsulated device with one side of the conductive traces exposed and available to provide electrical contact to the semiconductor device die. In forming the pattern of conductive traces on transfer film 12, for example by applying a layer of electrolytic copper foil to the transfer film, it is especially advantageous if the surface of the foil which is to contact the transfer film is smooth and the opposite side is rough. The smooth surface facilitates the peeling away of the transfer film after the encapsulation operation and the rough surface enhances the adherence of the resin material to the pattern of conductive traces.

FIG. 5 illustrates, again in cross section, the completed semiconductor device 30 after the transfer film has been removed. Device 30 includes semiconductor device die 15 which is enclosed within an encapsulating resin body 22. Exposed on one side of the resin body are portions of one side of the pattern of conductive traces 13. These conductive traces can be directly contacted for making electrical contact to the semiconductor device die. No thick device "header" or leadframe is necessary for mounting the device die, and so the thickness "t" is minimized. In addition to making contact to the conductive traces for the purpose of making electrical contact, some of the traces, such as trace 13 upon which device die 15 is mounted, can be contacted by a heat sink (not shown) in order to conduct heat away form the die during operation.

FIG. 6 illustrates, in cross section, a semiconductor device 32 in accordance with an alternate embodiment of the invention. This embodiment is similar to device 30 illustrated in FIG. 5 except that a protective coating 23 is applied to the exposed surface of the pattern of conductive traces 13. The protective coating can be, for example, a low temperature deposited oxide, polyimide, adhesively applied insulating film, or the like. Openings 24 are formed through insulating film 23 to expose selected portions of the pattern of conductive traces. Gold plating or other metallic plating can be applied to the exposed portions of the conductive traces to protect against corrosion of the those exposed portions and also to enhance the ability to electrically contact those portions. In device 32 only the contacts 24 are exposed and the rest of the semiconductor device is encapsulated either by encapsulating body 22 or by the protective film 23.

FIG. 7 illustrates schematically, in exploded view, a further embodiment of the invention. As illustrated in FIG. 7, an IC card structure or the like is fabricated by laminating a device such as device 30 between upper 40 and lower 42 plastic sheets. The three components are laminated together to form an IC card device 44. The term "IC card" is used to describe the debit cards and the like which incorporate an integrated circuit to update the financial or other status of the card as money is deposited or as the card is used. IC device 30 provides the intelligence included within the IC card. The flat plastic sheets 40, 42 provide a useful card size and include identifying information embossed on the faces as well as other information and user interface. The underside of sheet 40 may include a pattern of traces which interface with the pattern of traces 13 on device 30. The traces may be coupled together with solder bumps, conductive epoxy, or the like, or merely by the pressure of the lamination itself. Electrical contacts on the edge of one of the plastic sheets then provides an external electrical access to the device 30. Alternatively, device 30 itself, with a pattern as that illustrated in FIG. 5, may directly provide the external contact. For example, sheet 40 may be provided with a window or windows (not shown) which expose the pattern of traces on device 30 so that contact, for example by a card reader machine, can be made directly to those traces.

FIG. 9 illustrates, in plan view, the fabrication of semiconductor devices in accordance with a further embodiment of the invention in which a plurality of devices can be fabricated simultaneously. An elongated transfer film 50 provides a plurality of groups of patterns of conductive traces (parts of two groups are illustrated) on one surface thereof. The conductive traces are interconnected by a bus line 52 which allows the plurality of traces to be electrolytically plated. The patterns of conductive traces can be made, for example, by evaporating a film of conductive material onto the surface of elongated transfer film 50, patterning that evaporated film into the desired pattern, and then electroplating to achieve the desired thickness of conductive material. A semiconductor device die is mounted and interconnected to each of the groups of conductive traces and the die, interconnections, and one side of the conductive traces are encapsulated within a resin body 56. After the resin encapsulation, which is carried out in a manner similar to that described above, the elongated transfer film is peeled off or otherwise removed to expose the reverse side of the conductive traces. Either before or after the transfer film is removed, the traces can be severed along the lines 54 to electrically disconnect the individual devices so that they can be tested.

Thus it is apparent that there has been provided, in accordance with the invention, a semiconductor device and method for its fabrication which overcomes the

problems associated with the prior art devices and methods. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. For example, other patterns of conductive traces can be used and additional devices can be interconnected as needed. Additionally, other methods for forming both the conductive traces and for the encapsulation of the devices are possible. Thus it is intended to encompass within the invention all such variations and modifications as fall within the scope of the appended claims.

We claim:

1. A process for fabricating a semiconductor device comprising the steps of:

providing a transfer film;

providing a pattern of conductive traces on said transfer film;

providing a semiconductor device die;

forming electrical interconnections between said pattern of conductive traces and said semiconductor device die;

providing a resin material on one side of said transfer film to encapsulate said semiconductor device die, said electrical interconnections, and a portion of said pattern of conductive traces; and

removing said transfer film to expose one side of said pattern of conductive traces.

2. The process of claim 1 further comprising the step of forming a layer of insulating material over portions of said one side and leaving contact areas of said pattern exposed.

3. The process of claim 1 further comprising the step of laminating said semiconductor device die and said resin material between two sheets of plastic material.

4. The process of claim 3 wherein said step of laminating leaves exposed a portion of said one side.

5. The process of claim 4 further comprising the step of plating contact metal onto said exposed portion.

6. The process of claim 1 wherein said step of forming a pattern of conductive traces comprises the steps of:

forming a continuous layer of conductive material on said transfer film; and

selectively etching said continuous layer to form said pattern of conductive traces.

7. The process of claim 6 wherein said step of forming a continuous layer comprises laminating a layer of conductive foil to said transfer film.

8. The process of claim 6 wherein said step of forming a continuous layer comprises evaporating a layer of metal onto said transfer film.

* * * * *

Exhibit I

US005434739A

United States Patent [19]

Heck

[11] Patent Number: 5,434,739

[45] Date of Patent: Jul. 18, 1995

[54] **REVERSE BATTERY PROTECTION CIRCUIT**

[75] Inventor: **Karl R. Heck**, Phoenix, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **75,839**

[22] Filed: **Jun. 14, 1993**

[51] **Int. Cl.**[6] **H02H 3/18**

[52] **U.S. Cl.** **361/84**; 361/56

[58] **Field of Search** 361/84, 85, 92, 90, 361/56, 91, 77

[56] **References Cited**

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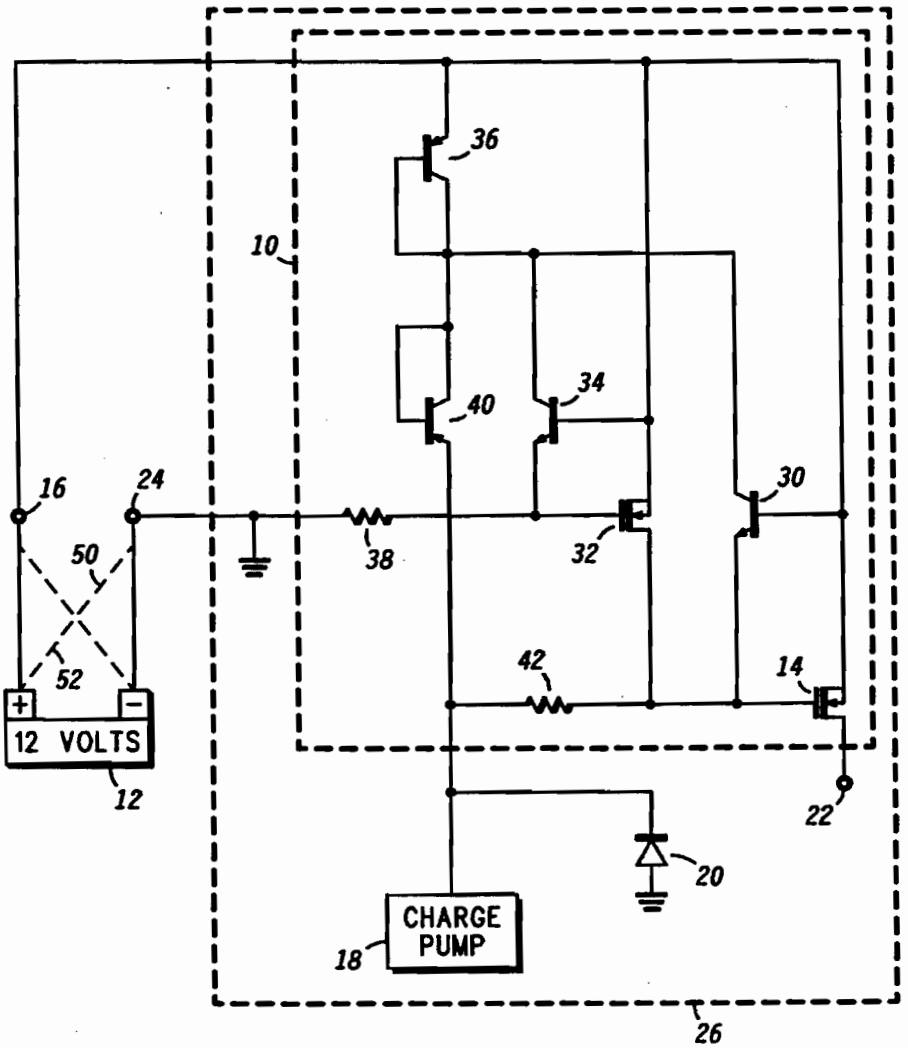
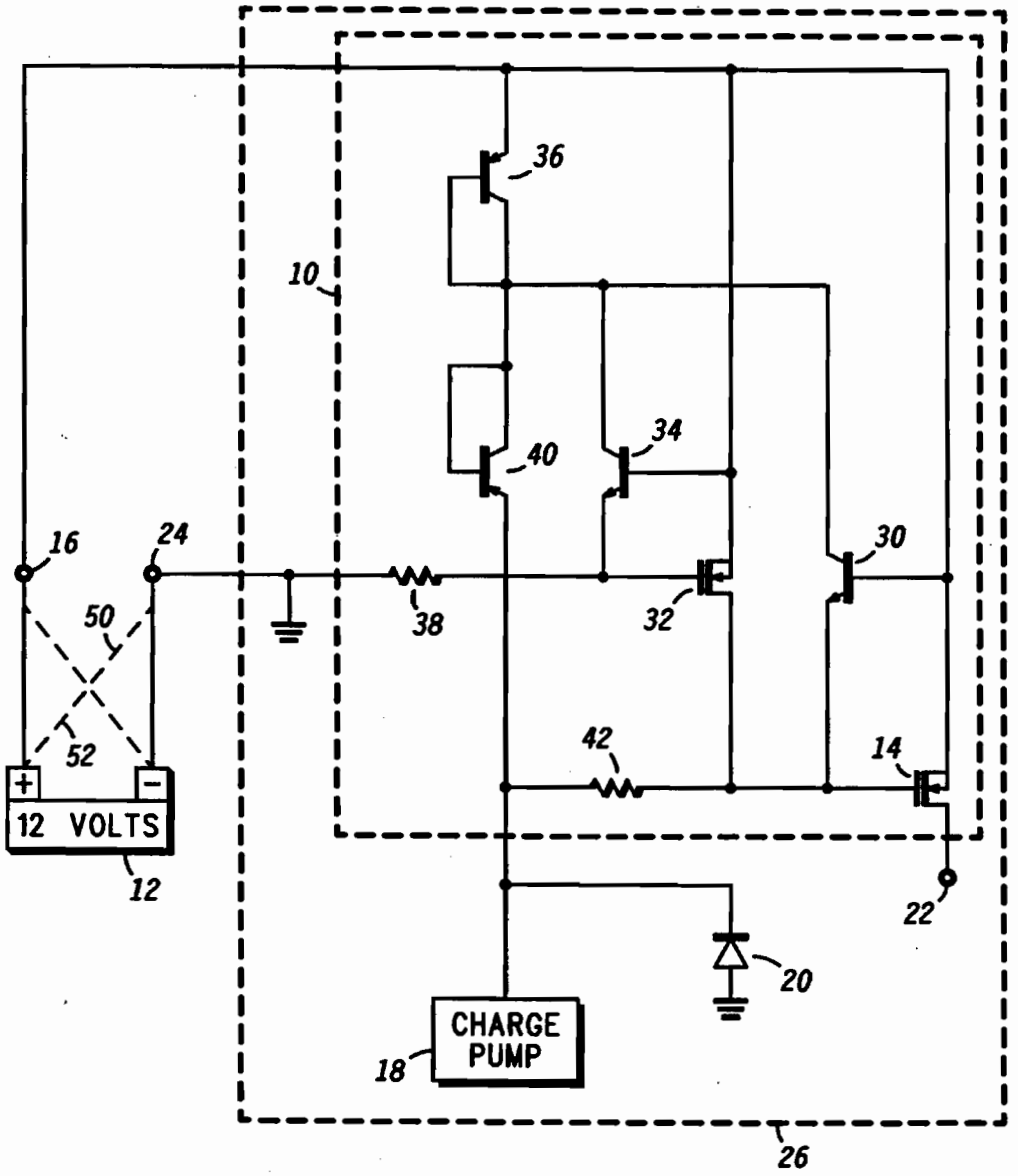
Primary Examiner—Marc S. Hoff
Assistant Examiner—S. Jackson
Attorney, Agent, or Firm—Rennie William Dover

[57] **ABSTRACT**

A protection circuit (**10**) for protecting internal circuitry of an integrated circuit (**26**) from a reverse battery connection has been provided. The protection circuit includes a pass transistor (**14**) which is rendered operative when the supply voltage is properly connected to the integrated circuit. However, when the power supply is improperly connected, a second transistor (**32**) becomes active thereby rendering the pass transistor inactive and not allowing the reverse supply voltage to be applied to the internal circuitry.

8 Claims, 1 Drawing Sheet

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CHARGE PUMP
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26

REVERSE BATTERY PROTECTION CIRCUIT

FIELD OF THE INVENTION

This invention relates to protection circuits and, in particular but not limited to, a reverse battery protection circuit for use in automotive applications.

BACKGROUND OF THE INVENTION

There currently exists a numerous types of electronic integrated circuits (IC's) for use in the automotive industry. Generally, the power supply for these circuits are generated from a 12-volt battery in an automobile. However, automotive IC's tied to the battery must survive the battery being hooked up backwards, for example, to avoid forward biasing epitaxial layers of the IC that are tied to the battery which thereby could result in destruction of the IC.

One attempt that prior art has made for providing reverse battery protection for IC's is to include a series diode between the battery and the integrated circuit wherein if the integrated circuit is connected to the battery backwards, the series diode is reversed biased and prevents supply voltage from being applied to the integrated circuit. However, the series diode solution compromises low voltage performance and the geometry of the diode becomes larger as supply current requirements increase.

Another attempt that prior art has made in providing reverse battery protection for an integrated circuit is to provide a saturated lateral PNP transistor in series between the battery and the integrated circuit. Although low voltage performance is not compromised in this solution, base current requirements for the lateral PNP increase power dissipation and the geometry of the PNP transistor becomes large as supply current requirements increase.

Another attempt that prior art has made in providing reverse battery protection for an integrated circuit is to provide a charged pumped reverse TMOS transistor as a pass device between the battery and the integrated circuit wherein the TMOS transistor has passive (resistive) gate to source termination. However, this solution requires DC current from the charge pump to enhance the TMOS transistor, and the turn off time of the TMOS transistor is limited by the size of the passive gate termination. Moreover, the charge pump must be high impedance when the supply voltage is reversed.

Hence, there exists a need for an improved reverse battery protection circuit for an integrated circuit that does not compromise low voltage performance, can efficiently handle moderate supply currents, does not demand DC current from a charge pump, and has a fast turn off time.

BRIEF DESCRIPTION OF THE DRAWING

The sole figure illustrates a detailed schematic diagram of a reverse battery protection circuit for protecting an integrated circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWING

Referring to the sole figure, there is illustrated reverse battery protection circuit **10** fabricated within integrated circuit (IC) **26** and being coupled between battery **12** and terminal **22**. It is understood that terminal **22** is further coupled to additional circuitry wherein this additional circuitry is desired to be protected from

reverse battery hook up. IC **26** includes protection circuit **10** as well as charge pump **18**, and any additional circuitry (not shown) coupled to terminal **22**. Terminal **24** is coupled to a ground reference of IC **26**.

Protection circuit **10** includes pass transistor **14** having a source electrode coupled to terminal **16** while the gate electrode of transistor **14** is coupled through resistor **42** to charge pump **18**. The back gate of transistor **14** is coupled to the source electrode of transistor **14** while the drain electrode of transistor **14** is coupled to terminal **22**.

Protection circuit **10** further includes transistor/zener diode **30** having a base coupled to terminal **16** and an emitter coupled to the gate electrode of transistor **14** and to the drain electrode of transistor **32**. The collector of transistor **30** is coupled to the collectors of transistor/zener diode **34** and transistor/diode **36** wherein the collector of transistor **36** is coupled to its base. The emitter of transistor **36** and the base of transistor **34** are both coupled to terminal **16**.

Moreover, the source electrode of transistor **32** and the back gate electrode of transistor **32** are coupled to terminal **16**. The emitter of transistor **34** is coupled to the gate electrode of transistor **32** and returned to ground through resistor **38**. The collector of transistor **34** is coupled to the collector of transistor/diode **40** wherein transistor **40** has its base coupled to its collector. The emitter of transistor **40** is coupled through resistor **42** to the gate electrode of transistor **14**. Moreover, the emitter of transistor **40** is coupled to charge pump **18**.

Charge pump **18** is coupled through diode **20** and returned to ground reference. In normal operation, transistor **14** requires the use of charge pump **18** to generate a voltage of at least 5 volts above a voltage supplied by battery **12**. Moreover, charge pump **18** is typically available on IC **26** since it is required for other applications.

Under proper connection, the positive terminal of battery **12** is coupled to terminal **16** while the negative terminal of battery **12** is coupled to terminal **24**. As a result, a positive supply voltage is applied to the source electrodes of transistors **32** and **14** as is desired. In this situation, transistor **14** is rendered operative while transistor **32** is rendered non-operative. As a result, the voltage appearing at terminal **22** (with respect to ground reference) will be substantially equal to the voltage appearing at terminal **16** (with respect to ground reference) less any IR drop occurring across transistor **14**.

However, if battery **12** is improperly hooked up in a reverse manner wherein the positive terminal of battery **12** is coupled to terminal **24** while the negative terminal of battery **12** is coupled to terminal **16** as represented by dotted lines **50** and **52**. This now means that a negative voltage (with respect to ground reference) is applied to the source electrodes of transistors **14** and **32** as is not desired. Under this condition, transistor **32** is rendered operative thereby shorting the gate electrode of transistor **14** to its source electrode and, thus, rendering transistor **14** non-operative. As a result, the voltage appearing at terminal **16** is not passed to terminal **22** and thus is not supplied to any additional internal IC circuitry. Further, any epitaxial layers typically coupled to terminal **22** cannot conduct current and damage integrated circuit **26**.

Transistor 30 functions as a zener diode to protect excessive voltage from appearing on the gate electrode of transistor 14. Essentially, the base of transistor 30 is the anode of the zener diode while the emitter of transistor 30 is the cathode of the zener diode. Moreover, the collector of transistor 30 is the third terminal of the zener diode and is coupled to the collector of transistor 34 which is the epitaxial island. Similarly, transistor 34 functions as a zener diode to protect excessive voltage from appearing on the gate electrode of transistor 32 wherein the base and emitters of transistor 34 respectively act as the anode and cathode of the zener diode while the collector of transistor 34 is coupled to the epitaxial island.

Moreover, resistor 38 functions to provide charge to render transistor 32 operative under a reverse battery condition. Also, resistor 42 functions to decouple the gate electrode of transistor 14 from charge pump 18.

It should be noted that components 30, 34, 32 and 38 are all fabricated in one epitaxial region which is biased by PNP transistors 36 and 40.

The present invention assures that no epitaxial islands are tied to terminal 16. As a result, if the connections of battery 12 are reversed, there are not epitaxial islands to be forward biased.

The present invention has several advantages. First, protection circuit 10 does not provide any additional DC loading on charge pump 18 when it is desired to enhance and turn on TMOS transistor 14. Second, under reverse battery conditions, charge pump 18 does not have to be heavily resistive or open for proper operation as is the case for prior art circuits. Thus, charge pump 18 does not have any special design requirements. Third, protection circuit 10 provides reverse battery protection without sacrificing power supply head room for low voltage operation since no series diodes are used. Moreover, the present invention quickly renders transistor 14 non-operative under a reverse battery condition. In particular, the discharge time constant for the gate electrode of transistor 14 is a product of the drain-source on resistance (R_{DSON}) of transistor 32 and the input capacitance (C_{ISS}) of transistor 14 which is substantially less than the turn off time for a passive gate termination scheme.

By now it should be apparent from the foregoing discussion that a novel protection circuit for protecting internal circuitry of an integrated circuit from a reverse battery connection has been provided. The protection circuit includes a pass transistor which is rendered operative when the supply voltage is properly connected to the integrated circuit. However, when the power supply is improperly connected, a second transistor becomes active thereby rendering the pass transistor inactive and not allowing the reverse supply voltage to be applied to the internal circuitry.

While the invention has been described in specific embodiments thereof, it is evident that many alterations, modifications and variations will be apparent to those skilled in the art. Further, it is intended to embrace all such alterations, modifications and variations in the appended claims.

I claim:

1. An integrated circuit having reverse battery protection, the integrated circuit including a charge pump and internal circuitry, the integrated circuit also including a protection circuit coupled between a first and second terminals wherein the first terminal is coupled to a battery and the second terminal is coupled to the internal circuitry, the protection circuit comprising:

a pass transistor having first and second current carrying electrodes and a control electrode, said first and second current carrying electrodes of said pass transistor respectively coupled between the first and second terminals, said control electrode of said pass transistor coupled to the charge pump;

a first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said control electrode of said pass transistor, said second current carrying electrode of said first transistor coupled to the first terminal;

a second transistor (30) having a collector, a base and an emitter, said base of said second transistor being coupled to the first terminal, said emitter of said second transistor coupled to said first current carrying electrode of said first transistor;

a third transistor (34) having a collector, a base and an emitter, said base of said third transistor coupled to the first terminal, said emitter of said third transistor coupled to said control electrode of said first transistor, said collector of said third transistor coupled to said collector of said second transistor;

a fourth transistor (40) having a collector, a base and an emitter, said collector of said fourth transistor coupled to said collector of said third transistor, said base of said fourth transistor coupled to said collector of said fourth transistor, said emitter of said fourth transistor coupled to said control electrode of said pass transistor;

a fifth transistor (36) having a collector, a base and an emitter, said collector of said fifth transistor coupled to said collector of said fourth transistor, said base of said fifth transistor coupled to said collector of said fifth transistor, said emitter of said fifth transistor coupled to the first terminal; and

a first resistor (38) coupled between said control electrode of said first transistor and a first supply voltage terminal.

2. The protection circuit according to claim 1 further including a second resistor (42) coupled between said emitter of said fourth transistor and said control electrode of said pass transistor.

3. A circuit for protecting internal circuitry of an integrated circuit from reverse battery connection, the integrated circuit including a charge pump and having first and second terminals coupled to a battery for supplying power to the integrated circuit, the circuit comprising:

first means for passing a voltage appearing across the first and second terminals to the internal circuitry when the integrated circuit is properly connected to the battery, said first means coupled between the first terminal and the integrated circuit and coupled to the charge pump;

second means for rendering said first means non-operative when the integrated circuit is improperly connected to the battery thereby blocking said voltage appearing across said first and second terminals from being passed to the internal circuitry, said second means including a first transistor which is rendered operative when the integrated circuit is improperly connected to the battery, said second means coupled between the first terminal and said first means.

4. The circuit according to claim 3 wherein said second means includes:

said first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said first means, said second current carrying electrode of said first transistor coupled to the first terminal;

a second transistor (30) having a collector, a base and an emitter, said base of said second transistor coupled to the first terminal, said emitter of said second transistor coupled to said first current carrying electrode of said first transistor;

a third transistor (34) having a collector, a base and an emitter, said base of said third transistor coupled to the first terminal, said emitter of said third transistor coupled to said control electrode of said first transistor, said collector of said third transistor coupled to said collector of said second transistor;

a fourth transistor (40) having a collector, a base and an emitter, said collector of said fourth transistor coupled to said collector of said third transistor, said base of said fourth transistor coupled to said collector of said fourth transistor;

a fifth transistor (36) having a collector, a base and an emitter, said collector of said fifth transistor coupled to said collector of said fourth transistor, said base of said fifth transistor coupled to said collector of said fifth transistor, said emitter of said fifth transistor coupled to the first terminal;

a first resistor (38) coupled between said control electrode of said first transistor and a first supply voltage terminal; and

a second resistor (42) coupled between said emitter of said fourth transistor and said first means.

5. The circuit according to claim 3 wherein said second means includes:

a first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said first means, said second current carrying electrode of said first transistor coupled to the first terminal;

first zener diode means (30) coupled across said second and control electrodes of said first transistor for limiting a voltage appearing thereacross; and

bias means coupled between the first terminal and said first means for biasing an epitaxial region in which said first transistor and said first zener diode means are fabricated.

6. The circuit according to claim 5 wherein said second means further includes second zener diode means (34) coupled across said first means for limiting a voltage appearing thereacross, said second zener diode means also being fabricated in said epitaxial region.

7. A method for providing reverse battery protection to internal circuitry of an integrated circuit, the integrated circuit having first and second terminals for coupling to a battery, the method comprising the steps of:

allowing a voltage appearing at the first terminal to pass through a transistor to the internal circuitry when the integrated circuit is properly coupled to the battery; and

actively disabling said transistor when the integrated circuit is improperly coupled to the battery thereby preventing said voltage appearing at the first terminal to pass to the internal circuitry.

8. An integrated circuit having reverse battery protection, the integrated circuit including a charge pump and internal circuitry, the integrated circuit also including a protection circuit coupled between first and second terminals wherein the first terminal is coupled to a battery and the second terminal is coupled to the internal circuitry, the protection circuit comprising:

a pass transistor having first and second current carrying electrodes and a control electrode, said first and second current carrying electrodes of said pass transistor respectively coupled between the first and second terminals, said control electrode of said pass transistor coupled to the charge pump; and

a first transistor for actively disabling said pass transistor when the battery is improperly connected thereby preventing a voltage appearing on the first terminal from appearing at the second terminal, said first transistor having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said control electrode of said pass transistor, said second current carrying electrode of said first transistor coupled to said first current carrying electrode of said pass transistor, said control electrode of said first transistor coupled to ground reference.

* * * * *

Exhibit J

US005476816A

United States Patent [19]

Mautz et al.

[11] Patent Number: 5,476,816

[45] Date of Patent: Dec. 19, 1995

[54] **PROCESS FOR ETCHING AN INSULATING LAYER AFTER A METAL ETCHING STEP**

[75] Inventors: **Karl E. Mautz**, Austin; **Jeffrey G. Cadenhead**, Kyle; **Thomas M. Allen**; **H. Adam Stevens**, both of Austin, all of Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **219,123**

[22] Filed: **Mar. 28, 1994**

[51] **Int. Cl.**[6] **H01L 21/44**

[52] **U.S. Cl.** **437/195**; 437/235; 156/653.1

[58] **Field of Search** 437/195, 235; 156/653.1; 148/DIG. 51

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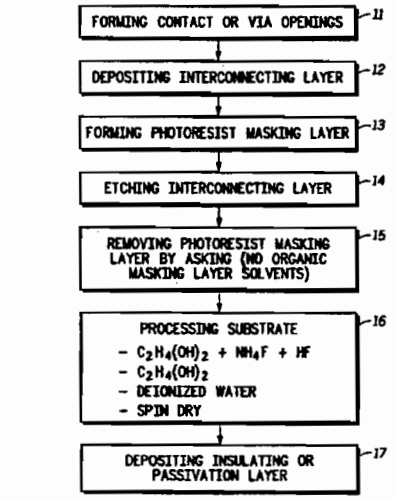
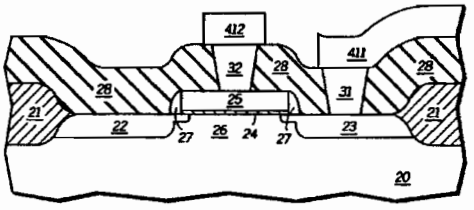
Primary Examiner—George Fourson
Assistant Examiner—C. Everhart
Attorney, Agent, or Firm—George R. Meyer

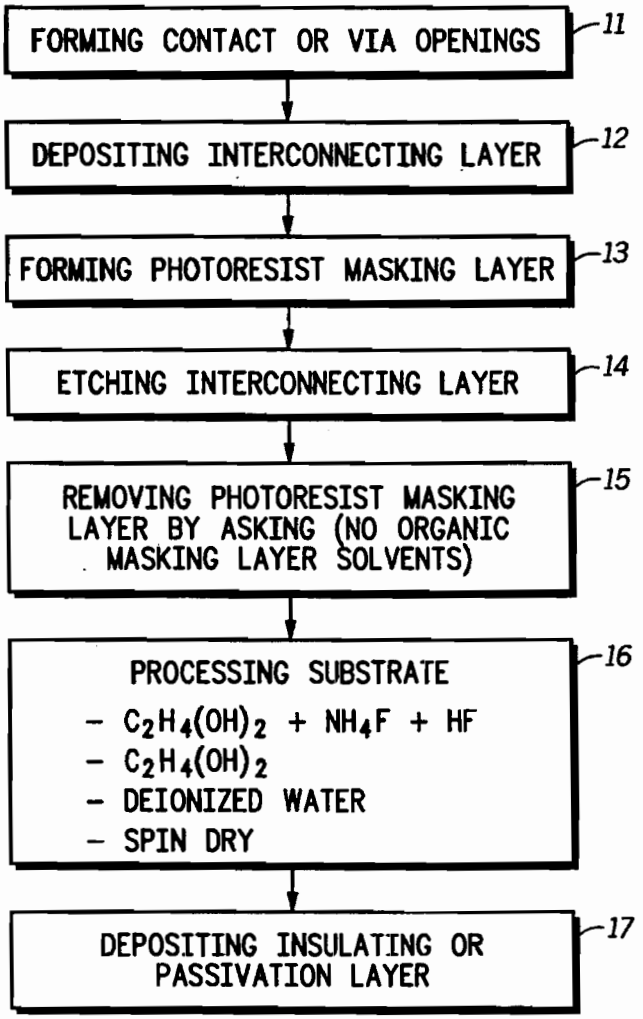
[57] **ABSTRACT**

A metal etch processing sequence eliminates the need to use an organic masking layer solvent and etches a portion of an insulating layer after a plasma metal etching step. The etch of the insulating layer is performed with an etching solution that may include 1,2-ethanediol, hydrogen fluoride, and ammonium fluoride. The etching solution etches in a range of 100–900 angstroms of the insulating layer. The etch removes at least 75 percent of the mobile ions within the insulating layer, and should remove at least 95 percent of the mobile ions. The process may be implemented using an acid hood, an acid compatible spray tool, or a puddle processing tool. The process includes many different embodiments that allow the process to be easily integrated into many different existing processing sequences. A similar process may be used with a resist-etch-back processing sequence.

21 Claims, 5 Drawing Sheets






FORMING CONTACT OR VIA OPENINGS
11
DEPOSITING INTERCONNECTING LAYER
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FORMING PHOTORESIST MASKING LAYER
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ETCHING INTERCONNECTING LAYER
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REMOVING PHOTORESIST MASKING LAYER BY ASKING (NO ORGANIC MASKING LAYER SOLVENTS)
15
PROCESSING SUBSTRATE
- $C_2H_4(OH)_2 + NH_4F + HF$
- $C_2H_4(OH)_2$
- DEIONIZED WATER
- SPIN DRY
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DEPOSITING INSULATING OR PASSIVATION LAYER
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FIG.1

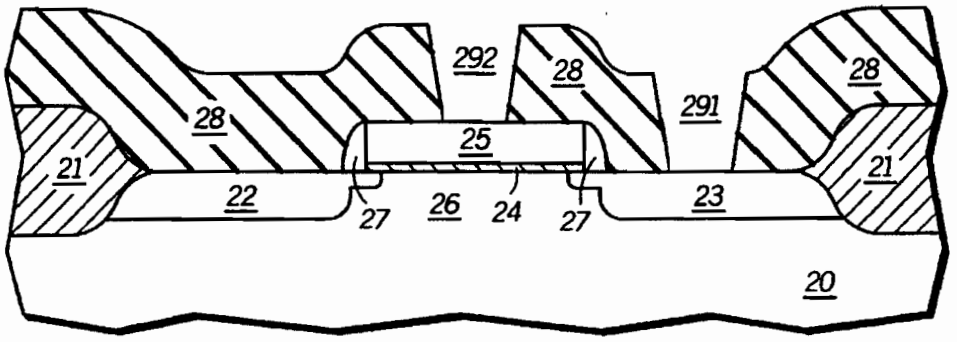
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FIG.2

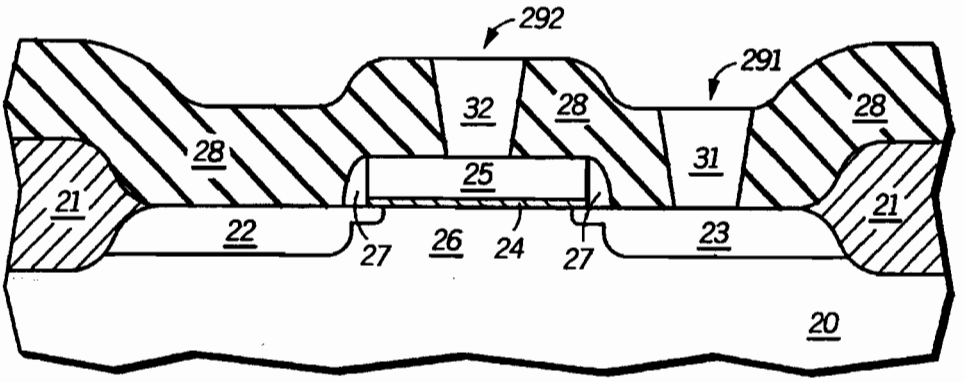

FIG.3

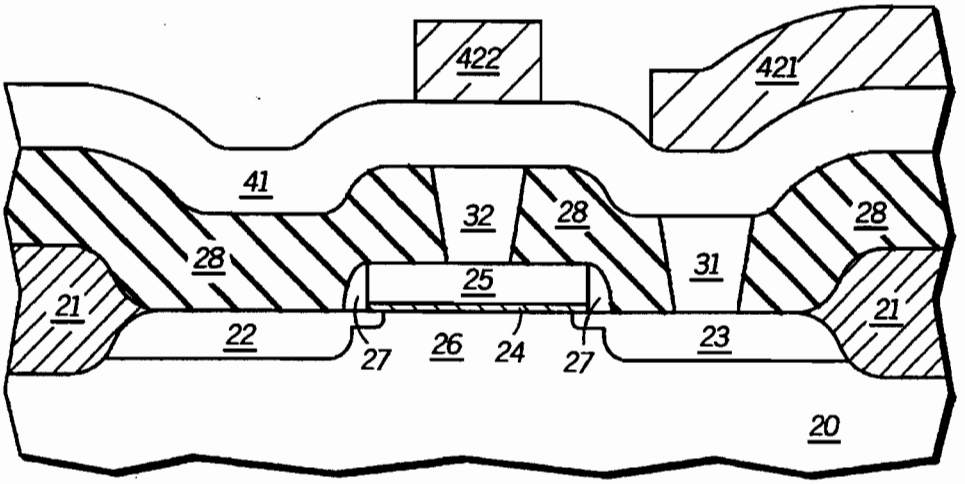

FIG.4

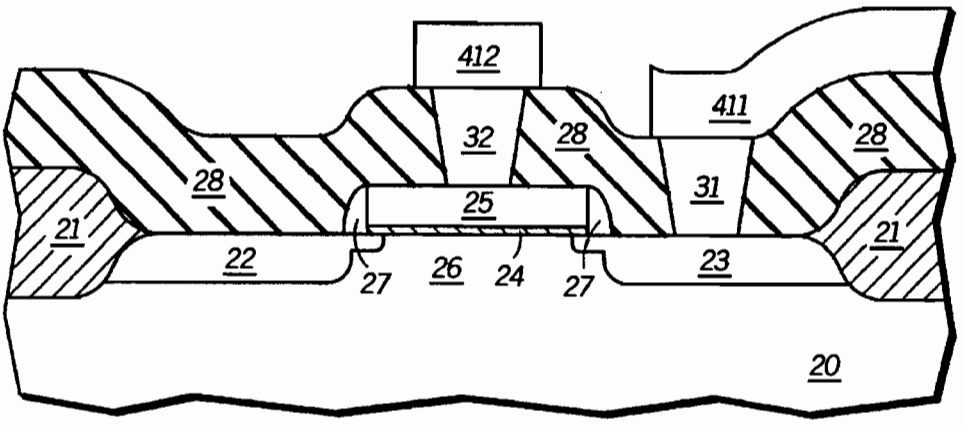

FIG.5

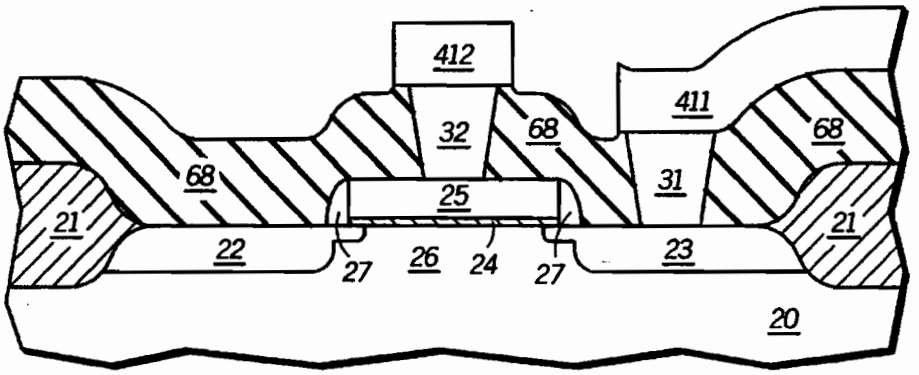

FIG.6

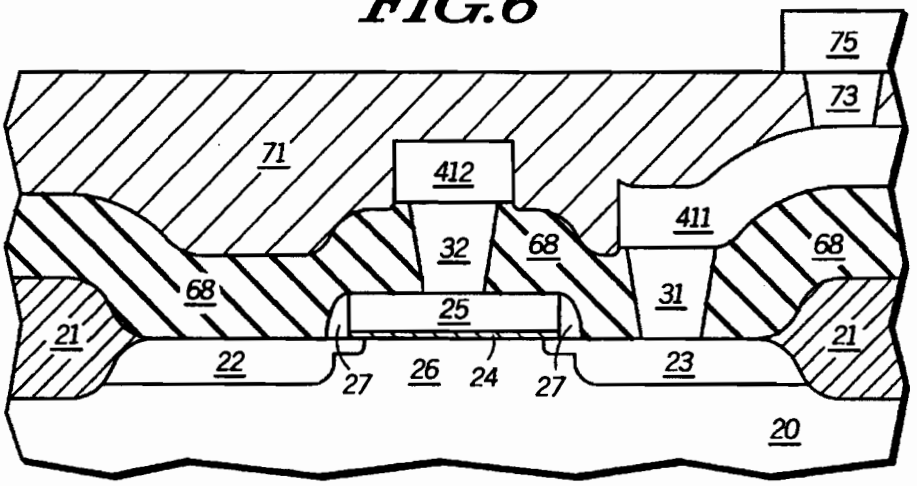

FIG.7

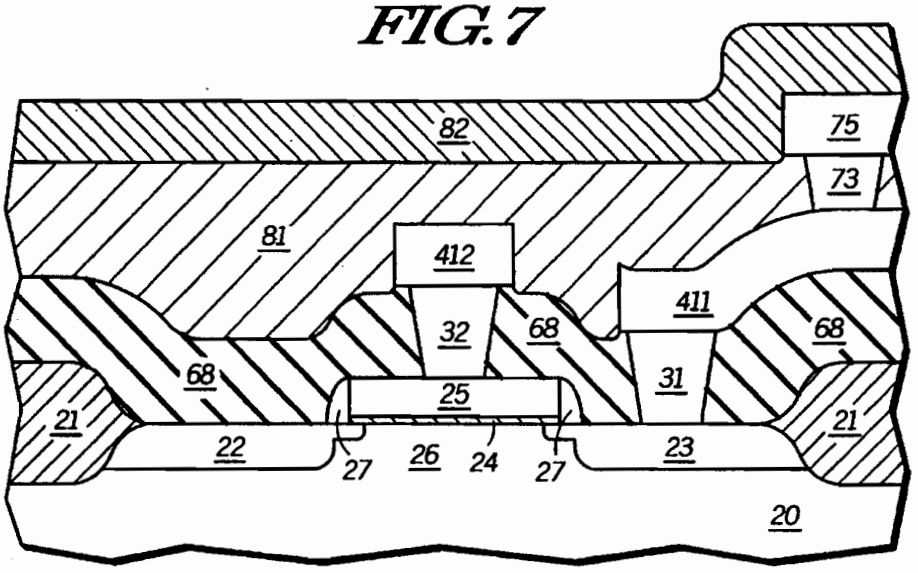

FIG.8

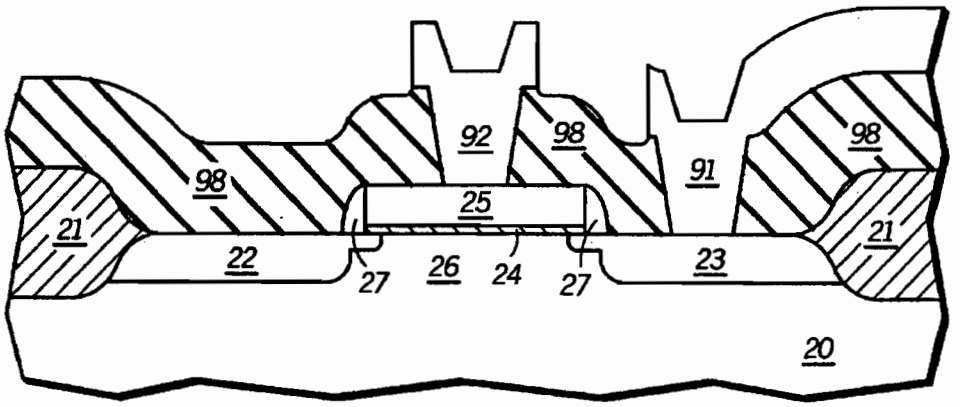

FIG.9

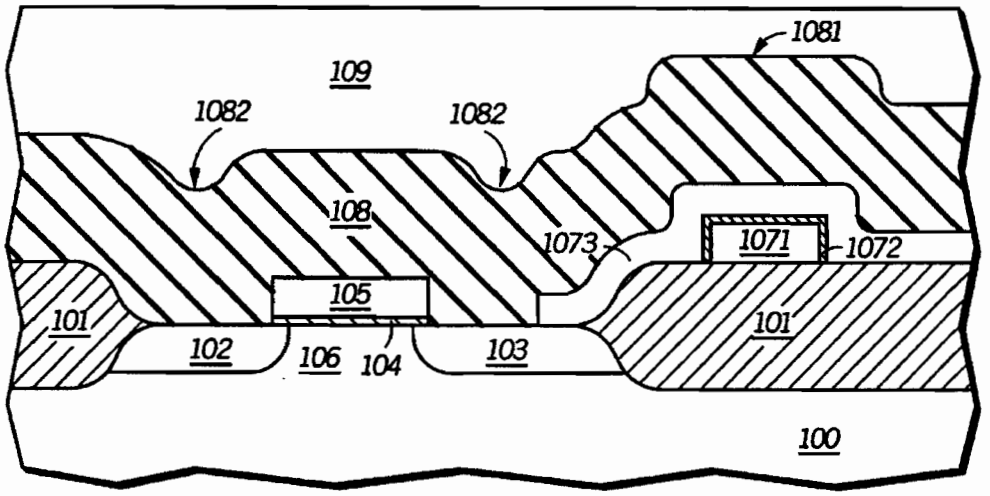

FIG.10

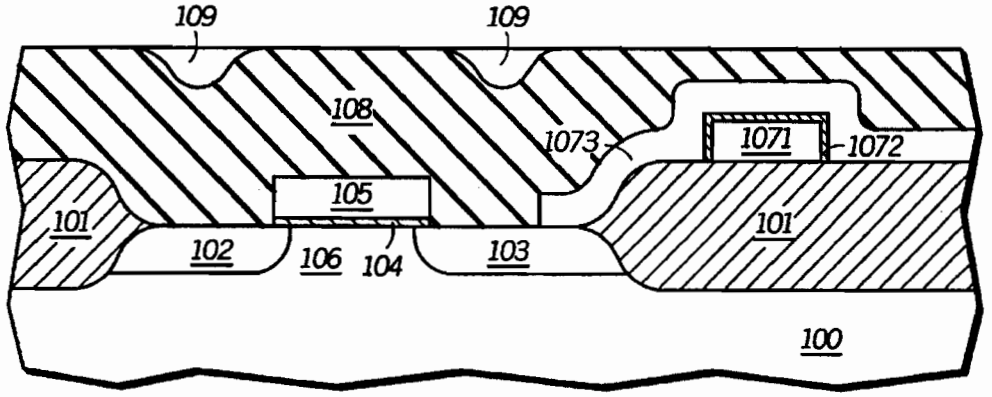

FIG.11

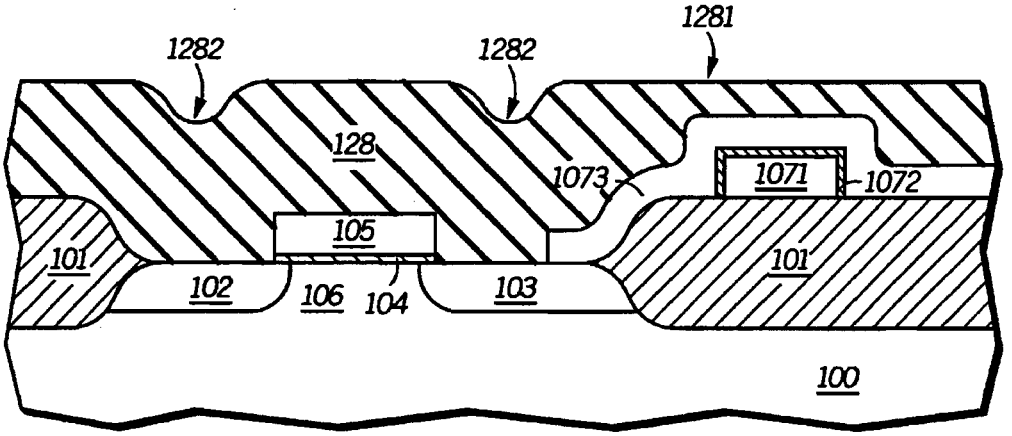
1281
1282
1282
128
1073
1071
1072
105
101
102
106
104
103
101
100

FIG.12

PROCESS FOR ETCHING AN INSULATING LAYER AFTER A METAL ETCHING STEP

FIELD OF THE INVENTION

The present invention relates to processes for forming semiconductor devices, and in particular, processes for forming insulating layers and interconnects in semiconductor devices.

BACKGROUND OF THE INVENTION

Interconnects allow various parts of a semiconductor device to be electrically connected with other parts of the semiconductor device. Unfortunately, the processes that form interconnects typically introduce mobile ions that degrade device reliability. Mobile ions, such as sodium, lithium, potassium, calcium, and magnesium, typically come from two sources: during a metal etching step and from an organic solvent typically used in removing a photoresist masking layer. The conventional wisdom of those skilled in the art is that mobile ions introduced during the metal etching steps lie only on exposed surfaces of an insulating layer or an interconnect formed during the metal etching process. A quick deionized water rinse after photoresist removal should remove virtually all of the mobile ions if they lie on exposed surfaces. Semiconductor devices that only have a deionized water rinse after photoresist removal still have unacceptably high device reliability problems.

Organic masking layer solvents include mobile ions. As used in this specification, an organic masking layer solvent is a chemical that is capable of readily removing an organic masking layer (i.e., photoresist, etc.). Examples of organic masking layer solvents include ketones (2-propanone (acetone), etc.), aliphatic hydrocarbons (n-heptane, etc.), alkali-amines (tetramethyl ammonium hydroxide, etc.), and aryl hydrocarbons (toluene, phenol, etc.). Examples of chemicals that are not organic masking layer solvents include alcohols (methanol, ethanol, 2-propanol (isopropyl alcohol), or the like) and glycols (methanediol (methylene glycol), 1,2-ethanediol (ethylene glycol), 1,2-propanediol (propylene glycol), or the like). These latter chemicals typically have at least one hydroxyl group for no more than ten carbon atoms within the molecule, wherein that hydroxyl group is directly attached to a carbon atom other than a carbon atom that is part of an aryl radical (i.e., not phenol). Although the alcohols and/or glycols may attack an organic masking layer, the rate of removing the organic masking layer typically is slow enough that it does not make the alcohols and/or glycols a chemical that readily removes an organic masking layer.

Many photoresist removal processes after a metal etching step use an organic masking layer solvent by itself or an aggregation of plasma ashing and an organic masking layer solvent. Many commercially-available organic solvents have mobile ions concentrations that are measured in parts per million. High-purity organic solvents are available that have mobile ions concentrations as low as about 10 parts per billion. However, these high purity organic solutions may still add mobile ion contamination to semiconductor devices. The cost of the organic solvents increase dramatically with higher purity.

Resist-etch-back processing sequences may also introduce mobile ions into a semiconductor device typically during a plasma etching step. Once again, mobile ions are undesired, and their concentration level in semiconductor devices should be kept as low as possible.

SUMMARY OF THE INVENTION

The present invention includes a process for forming a semiconductor device. The process of the present invention may comprise the steps of: forming a first insulating layer over a semiconductor substrate; depositing a metal-containing layer over the first insulating layer; forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions of the metal-containing layer; etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member; removing the patterned organic masking layer with a plasma gas and not with an organic masking layer solvent; etching a portion of the first insulating layer with a fluoride-containing solution; and forming a second insulating layer over the interconnect member. The step of etching the portion of the first insulating layer etches at least 100 angstroms of the first insulating or removes at least 75 percent of the mobile ions from the first insulating layer. The step of etching the portion of the first insulating layer is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

The process of the present invention may also comprise the steps of: forming a first insulating layer over a semiconductor substrate, wherein the first insulating layer includes a high point; forming an organic layer over the first insulating layer; simultaneously etching the organic layer and high point; etching a portion of the first insulating layer to a fluoride-containing solution; and rinsing the substrate after the step of etching the portion of the first insulating layer. The step of etching the portion of the first insulating layer etches at least 100 angstroms of the first insulating layer or removes at least 75 percent of the mobile ions from the first insulating layer. The step of etching the portion of the first insulating layer is performed after the step of simultaneously etching and prior to: 1) forming any layer over the first insulating layer; or 2) annealing the substrate including the first insulating layer.

Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limited to the figures of the accompanying drawing, in which like references indicate similar elements, and in which:

FIG. 1 includes a processing sequence of one embodiment to form a semiconductor device in accordance with the present invention.

FIG. 2 includes a cross-sectional view of a portion of a substrate after forming contact openings.

FIG. 3 includes the substrate of FIG. 2 after forming contact plugs.

FIG. 4 includes the substrate of FIG. 3 after forming an interconnecting level and photoresist members.

FIG. 5 includes the substrate of FIG. 4 after removing the photoresist members.

FIG. 6 includes the substrate of FIG. 5 after etching a portion of a first insulating layer after interconnects have been formed and prior to forming another layer over the first insulating layer and interconnects in accordance with the present invention.

FIG. 7 includes the substrate of FIG. 6 after forming a second insulating layer, a via plug, and an interconnect.

FIG. 8 includes the substrate of FIG. 7 after etching a portion of the second insulating layer and forming passivation in accordance with the present invention.

FIG. 9 includes the substrate of FIG. 2 after forming interconnects and etching a portion of the first insulating layer in accordance with the present invention.

FIG. 10 includes a cross-sectional view of a portion of a substrate prior to a resist-etch-back step.

FIG. 11 includes the substrate of FIG. 10 after etching a portion of an organic layer and a first insulating layer during a resist-etch-back step.

FIG. 12 includes the substrate of FIG. 11 etching a portion of a first insulating layer after the resist-etch-back step in accordance with the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

Embodiments of the present invention may be used to reduce mobile ion contamination that is introduced into a semiconductor device around the point in processing during steps of a metal etch processing sequence or a resist-etch-back processing step. Mobile ion contamination is believed to be introduced during the plasma metal etching step and during organic masking layer solvent processing for the plasma metal etching step. By eliminating the organic masking layer solvent and etching some of the insulating layer after the plasma metal etching step, mobile ion contamination introduced during the metal etch processing sequence may be substantially reduced. In resist-etch-back processing sequence, mobile ions may be introduced any time an organic layer and insulating layer are simultaneously etched. A portion of the insulating layer is etched to reduce the mobile ion concentration in the insulating layer. The present invention is better understood with the embodiments that are described below.

Interconnect Example

FIG. 1 includes a processing sequence used to form a semiconductor device. The processing sequence includes the steps of: forming contact or via openings 11; depositing an interconnecting layer 12; forming a photoresist masking layer 13; selectively etching the interconnecting layer 14; removing the photoresist masking layer by ashing (no organic masking layer solvents) 15; processing the substrate 16; and depositing an insulating layer 17.

FIG. 2 includes an illustration of a cross-sectional view of a portion of a semiconductor substrate 20. Field isolation regions 21, a source region 22, and a drain region 23 are formed from a part of the substrate 20 adjacent to its primary surface. The region of the substrate lying between the source and drain regions 22 and 23 and adjacent to the primary surface is a channel region 26. A gate dielectric layer 24 and a gate electrode 25 overlie the channel region 26 and a portion of the source and drain regions 22 and 23. Sidewall spacers 27 lie adjacent to the gate dielectric layer 24 and gate electrode 25, but the spacers 27 are not required. A first interlevel insulating layer 28 including silicon dioxide, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), or the like overlies the substrate 20 and includes a drain contact opening 291 and a gate contact opening 292. The first insulating layer 28 is about 8000 angstroms thick, but may be 4000– 20,000 angstroms thick in other embodiments. Conventional steps are used to form the device shown at this point in the process.

A drain contact plug 31 is formed within the drain contact opening 291, and a gate contact plug 32 is formed within the gate contact opening 292 as shown in FIG. 3. The contact plugs 31 and 32 may include tungsten; titanium; tantalum; a compound of tungsten, titanium or tantalum; or various combinations of these.

An interconnecting layer 41 and photoresist members 421 and 422 are formed over the first interlevel insulating layer 28 and contact plugs 31 and 32 as shown in FIG. 4. Exposed portions of the interconnecting layer 41 are formed where the photoresist members 421 and 422 do not overlie the interconnecting layer 41. The interconnecting layer 41 is a metal-containing layer and includes aluminum, aluminum with silicon, aluminum with copper, aluminum with silicon and copper, copper, or a copper alloy. The interconnecting layer 41 has a thicknesses in a range of 4000–50,000 angstroms. In alternate embodiments, a glue or barrier layer may be part of the interconnecting layer 41 or lie under or over the interconnecting layer 41. The glue or barrier layer may include titanium nitride, a titanium tungsten, or a titanium-tantalum and have a thickness in a range of 100–3000 angstroms. In addition, an anti-reflecting coating may be a part or overlie the interconnecting layer 41. The anti-reflecting coating may include a silicon layer, titanium nitride, a titanium-tungsten alloy, or a titanium-tantalum alloy and have a thickness in a range of 50–2000 angstroms. The glue layer, barrier layer, and/or anti-reflective coating (if any of the three are present) would be formed prior to forming the photoresist members 421 and 422.

The exposed portions of the interconnecting layer 41 (as seen in FIG. 4) are etched in a plasma reactor during a plasma metal etching step to form the first drain interconnect 411 and the gate interconnect 412 as shown in FIG. 5. The plasma metal etching step may be performed in a single substrate or batch reactor using reactive ion etching (RIE), or alternately using magnetically enhanced reactive ion etching (MERIE), electron cyclotron resonance (ECR), inductively coupled plasma versions (ICP), or helicon wave (HW) systems. The plasma metal etching step includes a breakthrough or stabilization portion, a main etch portion, an endpoint portion, and an overetch portion. The process may include a chlorine gas, such as molecular chlorine, boron trichloride, carbon tetrachloride, or silicon tetrachloride, any of which may used with or without an accessory gas, such as carbon tetrafluoride, trifluoromethane, nitrogen, helium, or argon. Optionally, bromine-based etchant gases of hydrogen bromide, boron tribromide, or other bromine gases may be substituted for the chlorine gas. During the various portions of the plasma metal etching step, a halide-containing plasma (usually a chlorine-containing plasma) is formed. Ions within the plasma do the actual etching of the exposed portions of the interconnecting layer 41.

During portions of the plasma metal etching step, typical operating pressures are in a range of 15–40 millitorr (204–544 millipascals), and typical radio-frequency powers are in a range of 750–2500 watts (or alternately expressed in terms of direct-current (dc) volts, in a range of minus 125 to minus 300 volts). The length of the breakthrough portion and the main etch portion are variable due to the thickness and composition of the interconnecting layer 41. The length of the endpoint portion is sufficient to detect when at least part of the interconnecting layer 41 has been removed over the first interlevel insulating layer 28.

The overetch portion has a large effect on the implantation of mobile ions into the interlevel insulating layer 28. This is

due to the interlevel insulating layer **28** being exposed to the ion bombardment of plasma ions and mobile ion contaminants within the plasma. The mobile ion contaminants typically accumulate on the plasma reactor inner surfaces as a result of etching the interconnecting layer **41** and the photoresist members **421** and **422** for this and other previously etched substrates having organic masking layers. These contaminants may become ionized during the plasma metal etching processing sequence. Typical parameters for the overetch portion utilizing batch reactors include pressures no less than 15 millitorr (204 millipascals) and no more than 40 millitorr (544 millipascals), radio-frequency power no less than 1250 watts and no more than 3000 watts, and dc bias no less then 220 volts and no more than 300 volts. The overetch portion length is highly variable. The length may range from 50–500 percent of the length of the endpoint step time, or can be expressed in terms of fixed time ranging from 100–900 seconds. In an alternate embodiment, single substrate reactors for the plasma metal etching step may be used. Other portions of the plasma metal etching step may be performed to prevent metal corrosion after the overetch portion of the plasma metal etching step.

After the plasma metal etching step, the photoresist members **421** and **422** may be removed using at least one conventional plasma ashing technique. The photoresist members **421** and **422** are substantially removed by the plasma ashing step. The photoresist members **421** and **422** are not removed in whole or in part by organic masking layer solvents. FIG. **5** is an illustration at this point in the process.

The first interlevel insulating layer **28** and interconnects **411** and **412** are rinsed with deionized water (optional), exposed to a fluoride-containing etching solution, and rinsed after being exposed to the etching solution. The etching solution typically includes hydrogen fluoride, ammonium fluoride, and a carrier solvent, such as 1,2-ethanediol. Within the etching solution, the hydrogen fluoride is in a range of 0.01–10 weight percent of the solution, ammonium fluoride is in a range of 1.0–50.0 weight percent of the solution, and 1,2-ethanediol makes up the remainder of the solution.

In alternate embodiments, alcohols or other glycols may be used. In general, the alcohols or glycols should have at least one hydroxyl group for every ten carbon atoms within the molecule, wherein that hydroxyl group is directly attached to a carbon atom other than a carbon atom that is part of an aryl radical. Further, the alcohol or glycol should be more viscous than water. The viscosity of the alcohol or glycol at 20 degrees Celsius is typically at least 2 centipoise. 1,2-ethanediol has a viscosity of about 20 centipoise at 20 degrees Celsius. The etching solution and rinsing solution are maintained at a temperature in a range of 20–50 degrees Celsius.

In another alternative embodiment, the hydrogen fluoride may be replaced by additional ammonium fluoride. In other alternate embodiments, the etching solution may include deionized water and/or carboxylic acids (such as acetic acid). The composition of the etching solution may be different when acetic acid is used compared to hydrogen fluoride. In still other embodiments, a surfactant may be included to reduce surface tension and improve the wetting properties of the solution. These wetting agents typically includes a perfluorosurfactant, a linear alkyl sulfonate, or an alkyl benzene sulfonate. For these other embodiments, the content of the components of the etching solution may vary from those previously given.

The solution etching step is designed to etch 100–900 angstroms of the first interlevel insulating layer **28**, and more typically 200–500 angstroms of first interlevel insulating layer **28**. The etching produces a "cleaned" first interlevel insulating layer **68** as shown in FIG. **6**. Various processing factor combinations can be used to form the cleaned first interlevel insulating layer **68**. These combinations are chosen for reasons of equipment stability, process stability, control of the removal rate of the first interlevel insulating layer **28**, or uniformity of the removal rate across the substrate surface. Specific details on the integration of the processing sequence to form the cleaned first interlevel insulating layer **68** may depend upon the equipment for which the processing sequence is integrated. The processing sequence may be performed in an acid hood, an acid-compatible spray tool, or a puddle processing tool. All of these pieces of equipment are known in the art, but the acid-compatible spray tool and the puddle processing tool are briefly described. The acid-compatible spray tool is similar to a spin rinse dryer (SRD) except that the acid-compatible spray tool has been modified to allow the use of acids. The puddle processing tool is a piece of equipment similar to a track used for coating photoresist onto a substrate except that the substrate is sent through at least one "puddle" of a chemical. The substrate is typically spun while it is in the puddle.

The process factors to produce the desired outputs (such as thickness of interlevel insulating layer removal and uniformity) for each equipment type are flexible. For acid hood processing, the exposure time to the etching solution is typically 60–120 seconds. The substrate cassette may or may not be agitated during this time. For the acid-compatible spray or puddle processing tool, the exposure time to the etching solution is typically 45–120 seconds. During the exposure, the substrate cassette or the substrate spin at a speed in a range of 20–75 revolutions per minute. The etching solution is fed into the acid-compatible spray tool or the puddle processing tool at a pressure in a range of 20–50 pounds per square inch (about 138–345 kilopascals) with a flow rate in a range of 0.5–2.5 gallons per minute (about 1.9–9.5 liters per minute). These factors affect the uniformity of the etching and the factors are set within these ranges to adjust for varying substrate sizes and surfaces. The temperature of the etching solution has a large effect on interlevel insulating layer removal rate and is typically 20–30 degrees Celsius.

In one embodiment, the rinsing of the substrate (after the exposure to the etching solution) may include an intermediate solvent rinse and then a deionized water rinse. The intermediate solvent rinse typically includes an alcohol or a glycol that is similar in type to the alcohol or glycol used with the etching solution. An example of the intermediate solvent includes 1,2-ethanediol. The intermediate solvent does not have to be the same solvent used in the etching solution, and therefore, the intermediate solvent may include 2-propanol, 1,2-propanediol, or the like. In alternate embodiments, the intermediate solvent may include deionized water and/or carboxylic acids (such as acetic acid). In still another embodiment, a surfactant may be included to improve the wetting of the intermediate solvent.

The solvent rinse is typically performed at a temperature in a range of 20–90 degrees Celsius. The intermediate solvent rinse time is in a range of 1–10 minutes. For the acid hood, the step may be performed in an overflow tank or quick dump rinser, with or without agitation. For the acid-compatible spray tool or the puddle processing tool, the substrate cassette or the substrate spins at a speed in a range of 25–100 revolutions per minute. For the acid-compatible spray tool or the puddle processing tool, the intermediate

solvent feed pressure and flow rate are typically about the same as the etching solution. The intermediate solvent rinse is followed by a deionized water rinse. The deionized water rinse process spins at a speed in a range of 25–300 revolutions per minute and the feed pressure and flow rate are typically about the same as the etching solution.

In alternate embodiments, additional deionized water rinses may be included. For example, the substrate may be rinsed with deionized water in a quick dump rinser and then be rinsed during a portion of a spin-rinse-dry cycle.

To maximize process integration, the etch using the fluoride-containing solution, intermediate solvent rinse, deionized water rinse, and drying the substrate may be performed sequentially all in as little as one cycle when using an acid-compatible spray tool. This type of process integration reduces cycle time and operator handling.

Further processing forms a second interlevel insulating layer **71**, a via plug **73**, and a second-level interconnect **75** as shown in FIG. **7**. The second interlevel insulating layer **71** may have the same or different composition as the first interlevel insulating layer **28** (as formed). Typically, the second interlevel insulating layer **71** includes an oxide. Although the second interlevel insulating layer **71** is illustrated to be planarized, in alternate embodiments, the second interlevel insulating layer **71** does not need to be planarized. Formation of the via plug **73**, and the second-level interconnect **75** are similar to the formation of the contact plugs **31** and **32** and the interconnects **411** and **412**, respectively.

After the second-level interconnect **75** is formed, the second interlevel insulating layer **71** is processed to form a "cleaned" second interlevel insulating layer **81** as shown in FIG. **8**. The processing to form the "cleaned" second interlevel insulating layer **81** uses a process meeting the criteria as described above with respect to the formation of the cleaned first interlevel insulating layer **68**. Still, the process to form the cleaned second insulating layer may or may not be the same as the process to form the cleaned first interlevel insulating layer **68**. A passivation layer **82**, which is an insulating layer, is formed over the cleaned second interlevel insulating layer **81** and the second-level interconnect **75** to form a substantially finished device as shown in FIG. **8**. Additional insulating layers, via plugs, and interconnecting layers, and other electrical connections may be made, if needed.

FIG. **9** includes an illustration of a cross-sectional view of an alternate embodiment. The alternate embodiment is similar to the one shown in FIG. **5** except that the combination of contact plugs and interconnects are replaced by interconnects **91** and **92**. Therefore, contact plugs are not required. Further processing is performed to form a substantially finished device. Processing with the acid hood, or acid-compatible spray tool, or puddle processing tool is done as described in previous figures to form a cleaned first interlevel insulating layer **98**. Similar to the interconnects **91** and **92**, the via plug **73** and second-level interconnect **75** (shown in FIG. **7**) may be replaced by a single interconnect.

Resist-Etch-Back Example

Some of the mobile ion and other device reliability problems similar to those described in the Interconnect Example may occur with a resist-etch-back process. FIG. **10** includes an illustration of a cross-sectional view of a portion of a semiconductor substrate prior to a resist-etch-back (REB) processing step. Field isolation regions **101**, source region **102**, drain region **103**, and channel region **106** lie at least partially within the substrate **100**. Gate dielectric layer **104** and gate electrode **105** overlie the channel region **106** and portions of the source and drain regions **102** and **103**.

A thin-film transistor overlies one of the field isolation regions **101** and includes a gate electrode **1071**, a gate dielectric layer **1072**, and an active layer **1073**. The active layer **1073** contacts the drain region **103**. A first insulating layer **108** overlies the thin-film transistor and other portions of the substrate **100** and has a composition similar to the first insulating layer **28** described above. The first insulating layer **108** includes high point **1081** and low points **1082**. The difference in elevation between the high point **1081** and low points **1082** may be more than one micron. Such a difference may cause problems with depositions of subsequent layers or lithographic steps. An REB processing sequence is typically performed to reduce the difference. The thin-film transistor may be replaced by another component, such as a metal interconnect or the like. In any event, a difference in elevation between the high and low points **1081** and **1082** of the first insulating layer **108** is too large and needs to be reduced. An organic layer **109**, such as a resist layer, overlies the first insulating layer **108**.

An REB step is performed to remove at least a portion of the organic layer **109** and a portion of the first insulating layer **108** as shown in FIG. **11**. The portion of the REB step in which the organic layer **109** and the first insulating layer **108** are simultaneously etched, has a large effect on the implantation of mobile ions into the first insulating layer **108**. This is due to a similar effect described in relation to overetch portion of the plasma metal etching step as previously described. Typical parameters for the simultaneous etching portion of the REB step when utilizing a batch reactor include pressures no less than 30 millitorr (408 millipascals) and no more than 70 millitorr (952 millipascals), radio-frequency power no less than 800 watts and no more than 1500 watts, and dc bias in a range of minus 350 volts to minus 500 volts, and gas flow ratios of a fluorine-containing gas (such as carbon tetrafluoride, trifluoromethane or the like) and oxygen, no less than one part fluorine-containing gas to one part oxygen and no more than four parts fluorine-containing gas to one part oxygen. The length of the REB step is highly variable. The length may be in a range of 10–60 minutes. The reactor cleanliness has a large effect on mobile ion implantation due to similar effects that were previously described in with respect to the overetch portion of the plasma metal etching step. In an alternate embodiment, a single substrate reactor for the REB step may be used.

The REB etching conditions are chosen, so that the first insulating layer **108** and the organic layer **109** etch at about the same rate. The etching rate of the first insulating layer **108** should be in a range of 0.5–2.0 times the etching rate of the organic layer **109**. During at least a portion of the REB step, both the first insulating layer **108** and organic layer **109** are simultaneously etched. Mobile ions are believed to become implanted into the first insulating layer **108** any time the first insulating layer **108** is exposed during the REB step. After the REB step, portions of the organic layer **109** and insulating layer **108** are present over the substrate **100**. In an alternate embodiment, the thickness of the first insulating layer **108** or REB etching conditions may be changed, so that all of the organic layer **109** is removed, and the first insulating layer **108** is planar. The REB step is performed to make the surface of the first insulating layer **108** more planar and typically does not form openings within the first insulating layer **108** (i.e., not a contact or via etching step).

Any remaining portions of the organic layer **109** are

removed by plasma ashing and without the use of organic masking layer solvents. In an alternate embodiment, the portions of the organic layer **109** may be removed by using organic masking layer solvents by themselves or with the plasma ashing step. The organic masking layer solvents may be used because interconnects or other layers are not exposed.

The first insulating layer is "cleaned" similar to the manner previously described in reference to the first interlevel insulating layer **28** of the Interconnect Example to form a cleaned first insulating layer **128** as shown in FIG. **12** that is similar to the cleaned first interlevel insulating layer **68** as seen in FIG. **6**. The cleaned first insulating layer **128** includes high point **1281** and low points **1282**. In an alternate embodiment, the first insulating layer may be cleaned in a megasonic sink having a dilute fluorine-containing solution, such as 50 parts deionized water to one part hydrofluoric acid, for example. Regardless of the equipment and chemicals used, the amount of the first insulating layer removed to form the cleaned first insulating layer **128** should meet the guidelines described previously with respect to the cleaned first insulating layer **68**.

The difference in elevation between the high and low points **1281** and **1282** is less than the difference in elevation between the high and low points **1081** and **1082** prior to the REB step. The difference is typically less than one micron, and more specifically is in a range of 100–3000 angstroms. The cleaning step of the REB Example is typically performed after the REB step and prior to: forming any other layer over the first insulating layer **108**; annealing the substrate including the first insulating layer **108**; or both.

Benefits

The embodiments of the present invention includes benefits. Mobile ions that are implanted into the insulating layer from the plasma metal etching step may be virtually eliminated by etching the surface of the insulating layer using an etching solution. The etching removes at least 75 percent of the mobile ions from the insulating layers and should remove at least 95 percent of all mobile ions from the insulating layers.

The concentration and depth of the mobile ions within an insulating layer depends on the plasma metal etching parameters that typically depend on the composition and thickness of the interconnecting layer. If any glue or barrier layers, or any anti-reflective coatings are present and etched, the plasma metal etching step may be performed under different parameters than if any of those layers are not present. Different plasma metal etching parameters may affect the concentration and depth of mobile ions within the insulating layer. The cleanliness of the plasma metal etching reactor in terms of mobile ions affects the concentration of same within the insulating layer.

As a result of the plasma etching process, organic masking layers and other polymer films incorporating mobile ions are consumed, releasing mobile ions into the plasma. The mobile ion levels within the reactor continue to increase during successive plasma metal etching cycles, causing higher concentrations of mobile ions to become implanted into an exposed insulating layer, until the interior reactor surfaces are disassembled and cleaned. Due to this accumulation, frequent disassembly and extensive cleaning of the reactor components is required, resulting in lost processing time. The embodiment of the present invention significantly reduces the frequency of cleaning required, and virtually eliminates the need for cleaning solely to reduce mobile ion concentrations within the plasma reactor.

The thickness range of the insulating layer to be removed to achieve the mobile ion reduction levels can be determined by analyzing the insulating layer after the plasma metal etching step is performed, prior to and after solution etching the insulating layer. The analysis can be performed by secondary ion mass spectrometry (SIMS) or equivalent to determine the concentration of mobile ions in the insulating layer. This technique uses an energetic beam of primary ions to sputter away secondary ions from a solid sample. Secondary ions of a given mass to charge ratio may then be plotted as a function of sputtering time. The raw data does not necessarily provide information on the ionic concentration as a function of depth. Due to the energetic effects of SIMS analysis, movement of the ions through the insulating layer occurs and this affects the ions' position during the depth profile, compared to the ions' position prior to the analysis. The total integral of the depth profile does provide mobile ion reduction information by comparison. If known thicknesses of oxide are removed by solution etching the insulating layer prior to SIMS depth profiling, the remaining fraction of the mobile ions can be measured by integration to determine the difference. Etching of oxide thicknesses less than 100 angstroms may result in less than a 75 percent reduction of mobile ions in the insulating layer. Etching of oxide thickness greater than 900 angstroms typically results in no further significant reduction in mobile ion concentration and may cause other problems that are not related to mobile ions. For most mobile ion reduction applications, between 200–500 angstroms of the insulating layer is etched with a fluoride-containing solution after the plasma metal etching step.

Benefits in mobile ion reduction occur with the REB Example, too. Any reduction in mobile ions generally improves device reliability. The amount and depth of mobile ions in the first insulating layer **108** depends on the etching parameters during the REB step. The determination of how much of the first insulating layer **108** is to be etched during the cleaning step may be performed by a SIMS analysis similar to the one described above. Removal of oxide thicknesses less than 100 angstroms may result in less than a 75 percent reduction of mobile ions in the insulating layer. Removal of oxide thickness greater than 900 angstroms typically results in no further significant reduction in mobile ion concentration and may cause other problems that are not related to mobile ions. For most mobile ion reduction applications, between 200–500 angstroms of the insulating layer are solution etched after the REB step.

Another benefit is that organic masking layer solvents are not required. Many of these organic masking layer solvents (particularly alkali-amine solvents) include mobile ions that are present at a concentration of at least 10 parts per billion. Although this is a low concentration, it is large enough to cause device reliability problems. It is believed that the mobile ions present in the solvent may attach to exposed surfaces of the interconnects that may have some residual chlorine, and can attract the mobile ions thereby increasing the mobile ion concentration in the device. High mobile ion concentrations are known to reduce device performance and reliability.

The other advantages of the embodiments of the present invention include virtually complete removal of non-ashable residues and less interconnecting layer damage. Residue removal typically requires exposure to the organic masking layer solvents, such as alkali-amine solvents, to remove these residues. With the exposure to the organic masking

layer solvents, mobile ion additions to the device are almost guaranteed. The etching solution dissolves the residues, as opposed to organic masking layer solvents that break the structures into smaller parts. The etching solution (described in the embodiments above) lowers the adhesion of the residues to the interconnects. Organic masking layer solvents damage interconnects, and the damage may include pitting of the interconnect due to electrolytic dissolution and roughening of the surfaces due to grain removal. Because organic masking layer solvents are not used, the embodiments of the present invention have less damage to the surfaces of the interconnects.

The embodiments of the present invention may require less processing time and less chemicals per cycle compared to organic masking layer solvent processes. The chemicals used in the embodiments described above contain less particles and inherently cause less defectivity. This results in cleaner processing, improved device performance and yield. Separate steps of post-metal etch deionized water rinsing and chemical solution cleaning may be combined into one equipment cycle, reducing processing and staging time, and needed equipment. The use of glycol or alcohol chemicals as a carrier solvent is an advantage due to their higher viscosity than the etchant chemical. This acts as a passivant to protect the interconnect surfaces from excess exposure to the etchant chemical, preventing corrosion and other damage to the interconnects.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. However, it will be evident that various modifications and changes can be made thereto without departing from the broader spirit or scope of the invention as set forth in the appended claims. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A process for forming a semiconductor device comprising the steps of:

forming a first insulating layer over a semiconductor substrate;

depositing a metal-containing layer over the first insulating layer;

forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions of the metal-containing layer;

etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member;

removing the patterned organic masking layer with a plasma gas;

etching a portion of the first insulating layer with a fluoride-containing solution, wherein this step:

etches at least 100 angstroms of the first insulating layer; and

is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

forming a second insulating layer over the interconnect member.

2. The process of claim 1, wherein the step of etching the portion of the first insulating layer etches at least 75 percent of mobile ions from the first insulating layer.

3. The process of claim 1, wherein the fluoride-containing solution includes:

hydrogen fluoride;

ammonium fluoride; and

a chemical selected from a group consisting of an alcohol and a glycol.

4. The process of claim 1, wherein the fluoride-containing solution is at a temperature in a range of 20–50 degrees Celsius.

5. The process of claim 1, wherein the step of etching the portion of the first insulating layer etches in a range of 200–500 angstroms of the first insulating layer.

6. The process of claim 1, further comprising a step of rinsing the substrate with deionized water between the steps of etching the exposed portions of the metal-containing layer and etching the portion of the first insulating layer.

7. The process of claim 1, further comprising steps of:

rinsing the substrate with a chemical selected from a group consisting of an alcohol and a glycol before rinsing the substrate with deionized water;

rinsing the substrate with deionized water; and

drying the substrate,

wherein the steps of rinsing the substrate with a chemical, rinsing the substrate with deionized water, and drying the substrate are performed between the steps of etching the portion of the first insulating layer and forming a second insulating layer.

8. The process of claim 7, wherein the steps of etching the portion of the first insulating layer, rinsing the substrate with the chemical, rinsing the substrate with deionized water, and drying the substrate are performed in an acid-compatible spray tool during the same cycle.

9. A process for forming a semiconductor device comprising the steps of:

forming a first insulating layer over a semiconductor substrate;

depositing a metal-containing layer over the first insulating layer;

forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions of the metal-containing layer;

etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member;

removing the patterned organic masking layer with a plasma gas;

etching a portion of the first insulating layer with a fluoride-containing solution, wherein this step:

removes at least 75 percent of mobile ions from the first insulating layer; and

is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

forming a second insulating layer over the interconnect member.

10. The process of claim 9, wherein the step of etching the portion of the first insulating layer etches in a range of 200–500 angstroms of the first insulating layer.

11. The process of claim 9, wherein the fluoride-containing solution includes:

hydrogen fluoride;

ammonium fluoride; and

a chemical selected from a group consisting of an alcohol and a glycol.

12. The process of claim 9, wherein the fluoride-containing solution is at a temperature in a range of 20–50 degrees Celsius.

13. The process of claim 9, further comprising a step of rinsing the substrate with deionized water between the steps of etching the exposed portions of the metal-containing layer and etching the portion of the first insulating layer.

14. The process of claim 9, further comprising steps of:

rinsing the substrate with a chemical selected from a group consisting of an alcohol and a glycol before rinsing the substrate with deionized water;

rinsing the substrate with deionized water; and

drying the substrate,

wherein the steps of rinsing the substrate with a chemical, rinsing the substrate with deionized water, and drying the substrate are performed between the steps of etching the portion of the first insulating layer and forming a second insulating layer.

15. The process of claim 14, wherein the steps of etching the portion of the first insulating layer, rinsing the substrate with the chemical, rinsing the substrate with deionized water, and drying the substrate are performed in an acid-compatible spray tool during the same cycle.

16. The process of claim 1, wherein an organic masking layer solvent is not used to remove the patterned organic masking layer.

17. The process of claim 1, wherein the fluoride-containing solution includes a carrier solvent that has a viscosity of at least 2 centipoise at 20 degrees Celsius.

18. The process of claim 7, wherein:

the fluoride-containing solution includes a carrier solvent; and

each of the carrier solvent and the chemical for rinsing the substrate has a viscosity of at least 2 centipoise at 20 degrees Celsius.

19. The process of claim 9, wherein an organic masking layer solvent is not used to remove the patterned organic masking layer.

20. The process of claim 9, wherein the fluoride-containing solution includes a carrier solvent that has a viscosity of at least 2 centipoise at 20 degrees Celsius.

21. The process of claim 14, wherein:

the fluoride-containing solution includes a carrier solvent; and

each of the carrier solvent and the chemical for rinsing the substrate has a viscosity of at least 2 centipoise at 20 degrees Celsius.

* * * * *

Exhibit K

US005593538A

United States Patent [19]

Davison et al.

[11] Patent Number: 5,593,538

[45] Date of Patent: Jan. 14, 1997

[54] **METHOD FOR ETCHING A DIELECTRIC LAYER ON A SEMICONDUCTOR**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **537,053**

[22] Filed: **Sep. 29, 1995**

[51] **Int. Cl.**[6] **H01L 21/311**

[52] **U.S. Cl.** **156/637.1**; 156/656.1; 156/626.1; 156/642.1; 216/90; 216/84; 216/93

[58] **Field of Search** 216/57, 83, 96, 216/86; 156/657.1, 662.1, 642.1

[56] **References Cited**

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Primary Examiner—R. Bruce Breneman

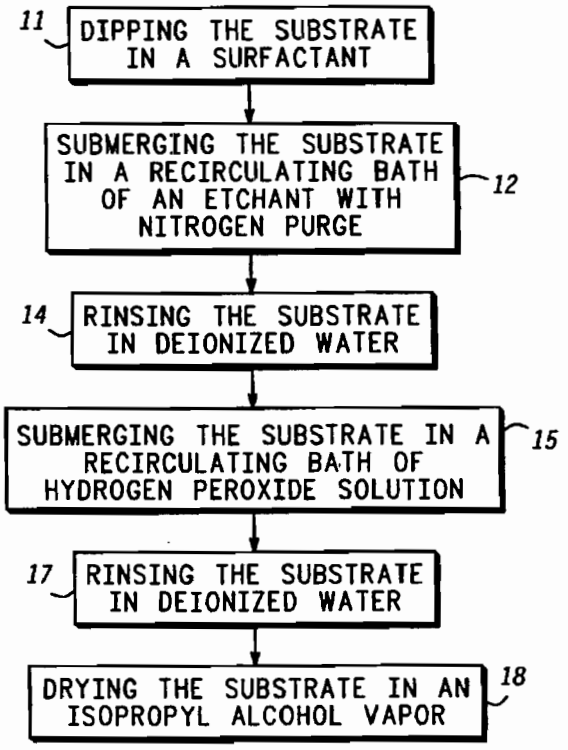
Assistant Examiner—Michael E. Adjodha

Attorney, Agent, or Firm—Rennie William Dover

[57] **ABSTRACT**

A wet etching process (**10**) etches sacrificial oxide on a substrate without damaging a polycrystalline silicon structure on the substrate. The etching process (**10**) includes dipping the substrate in a surfactant (**11**), submerging a portion of the substrate in a recirculating bath of the etchant while injecting an inert gas into the etchant (**12**) to purge the etchant of oxygen, rinsing the substrate in deionized water (**14**), submerging a portion of the substrate in a hydrogen peroxide solution (**15**), rinsing the substrate for a second time (**17**), and drying the substrate in isopropyl alcohol vapor (**18**). The inert gas injected into the etchant displaces oxygen dissolved in the etchant and protects the polycrystalline silicon structure from being etched.

20 Claims, 1 Drawing Sheet



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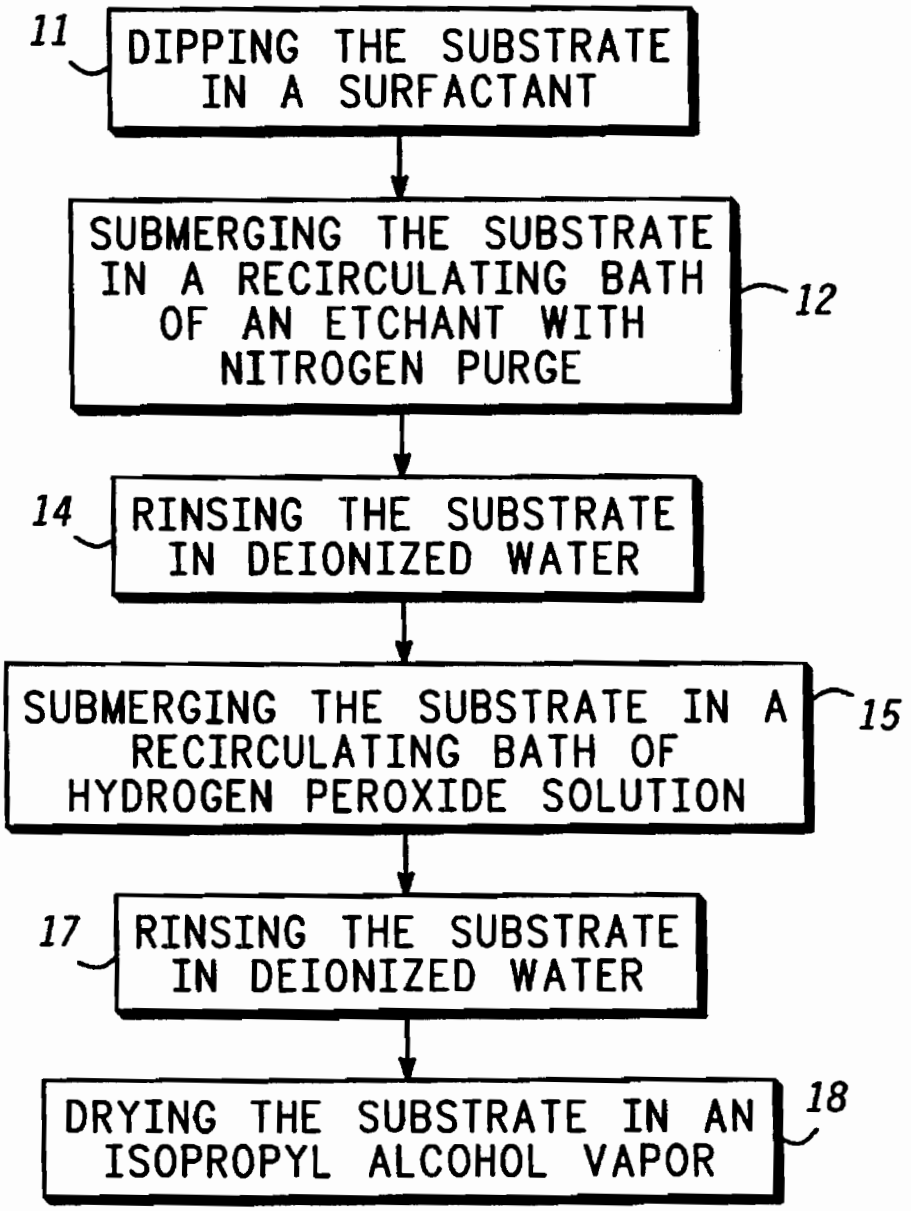
11
DIPPING THE SUBSTRATE IN A SURFACTANT
SUBMERGING THE SUBSTRATE IN A RECIRCULATING BATH OF AN ETCHANT WITH NITROGEN PURGE
12
14
RINSING THE SUBSTRATE IN DEIONIZED WATER
SUBMERGING THE SUBSTRATE IN A RECIRCULATING BATH OF HYDROGEN PEROXIDE SOLUTION
15
17
RINSING THE SUBSTRATE IN DEIONIZED WATER
DRYING THE SUBSTRATE IN AN ISOPROPYL ALCOHOL VAPOR
18
10

METHOD FOR ETCHING A DIELECTRIC LAYER ON A SEMICONDUCTOR

BACKGROUND OF THE INVENTION

The present invention relates, in general, to etching a substrate, and more particularly, to etching a dielectric material over a semiconductor material.

Wet etching is widely used in semiconductor processing for removing dielectric material, e.g., oxide, from a semiconductor wafer. In one wet etching process, an etchant such as a six to one buffered oxide etchant (6:1 BOE), which consists of six parts of ammonia fluoride and one part of hydrogen fluoride, is used to etch an oxide layer, such as a phosphorus doped silicate glass (PSG) layer, on a semiconductor wafer. The process starts with dipping the semiconductor wafer into a surfactant. The semiconductor wafer is then submerged into a recirculating bath of the etchant to etch the sacrificial oxide. After etching, the semiconductor wafer is rinsed in deionized water and then dried in an isopropyl alcohol vapor. In some applications, e.g., in sensor applications, the semiconductor wafer is submerged in a hydrogen peroxide solution after it is rinsed in the deionized water, followed by a second deionized water rinse before being dried in the isopropyl alcohol vapor.

If the semiconductor wafer includes a conductive structure such as a polycrystalline silicon structure, the polycrystalline silicon structure is exposed to the etchant after the sacrificial oxide is etched away. The etchant etches the polycrystalline silicon, wherein the extent of the etching is dependent on the composition and temperature of the etchant as well as the duration of the etching process. If the polycrystalline silicon is structured as thin conductive lines electrically connecting different components on the semiconductor wafer, the etching process can create open circuits in some areas on the wafer. The etching process also creates reliability problems when a polycrystalline silicon line is etched to a very thin line because a thin line cannot carry the current required for the circuit in the semiconductor wafer to perform properly.

Accordingly, it would be advantageous to have a process for etching a dielectric material over a semiconductor wafer that does not damage a conductive structure on the wafer. It would be of further advantage for the etching process to be simple and easily integrated into an existing etching process.

BRIEF DESCRIPTION OF THE DRAWING

The sole FIGURE is a flow chart of an etching process in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWING

Generally, the present invention provides a method for etching a substrate. More particularly, the present invention provides a wet etching process for an oxide layer on a semiconductor material.

In a wet etching process in accordance with a prior art embodiment, polycrystalline silicon is etched when it is exposed to an etchant. The etching of the polycrystalline silicon may cause open polycrystalline silicon lines in some areas as well as reliability problems by creating very thin polycrystalline silicon lines. An objective of the present invention is to provide an etching process that does not etch a conductive structure such as, for example, a polycrystalline silicon structure, on a semiconductor wafer. Through an extensive investigation, it has been discovered that the

etching of the polycrystalline silicon structure is caused by oxygen dissolved in the etchant. Therefore, the present invention provides a method for protecting the conductive structure on a substrate during a wet etching process by purging away oxygen dissolved in the etchant.

The sole FIGURE is a flow chart **10** of an etching process in accordance with an embodiment of the present invention. To protect a conductive structure, e.g., a polycrystalline silicon structure, on the substrate during the etching process, an inert gas such as, for example, nitrogen gas is injected into the etchant. The injected inert gas protects the polycrystalline silicon on the semiconductor wafer by purging away or displacing the oxygen dissolved in the etchant. In other words, the injected inert gas serves as a purgative gas to purge the etchant of oxygen, thereby forming a purged or degassed etchant. Other gases suitable for serving as the purgative gas to be injected into the etchant include carbon dioxide, helium, neon, argon, krypton, xenon, and the like.

The etching process illustrated by flow chart **10** is suitable for etching a dielectric material such as a sacrificial oxide from a substrate such as, for example, a semiconductor wafer. Commonly used sacrificial oxides in semiconductor industry include phosphorus doped silicate glass, tetra methyl phosphite, and the like.

In a first step **11**, the substrate is dipped in a surfactant for a time period such as, for example, one minute. By way of example, the surfactant is a poly oxyalkylene alkylphenyl ether aqueous solution sold under trademark NCW 601A by Waco Chemical.

In a second step **12**, a portion of the substrate is submerged in a recirculating bath of an etchant such as, for example, a six to one buffered oxide etchant (6:1 BOE) consisting of six parts of ammonia fluoride and one part of hydrogen fluoride. The temperature of the etchant and the substrate submersion time will determine the extent of the etching. In one example, the temperature of the etchant is set at 35 degrees Celsius (°C.) and the substrate is submerged in the etchant for 70 minutes. An inert gas such as, for example, nitrogen gas, is injected into the etchant to purge the etchant of the oxygen. In one approach, the inert gas is injected while the etchant is flowing in a recirculating path. In the approach, a tub having at least one injector installed at the bottom of the tub is filled with the etchant. To achieve a uniform etching environment in the tub, several injectors are preferably installed at the bottom of the tub with the injectors evenly distributed throughout the bottom of the tub. Recirculation of the etchant is established by overfilling the tub with the etchant. The portion of the etchant that overflows the tub is collected in a recirculating path, pumped through a filter, and injected back into the tub via the injectors. The inert gas is injected into the etchant in a direction opposite to the flow of etchant along the recirculating path. This approach ensures that a maximum amount of the inert gas is dissolved in the etchant. The inert gas dissolved in the etchant displaces the oxygen and protects the polycrystalline silicon structure from being etched. It is usually preferred to inject the inert gas into the etchant throughout the whole etching process. However, this is not always necessary. The inert gas can be injected into the etchant to purge away the oxygen prior to the etching process. It should be understood that the composition and the temperature of the etchant, and the length of the etching process are not limited to the values described supra. These parameters can be adjusted to optimize each etching process. It should also be understood that the protection provided by the injected inert gas is not limited to a polycrystalline silicon structure. Any structure on the substrate that reacts

with the oxygen dissolved in the etchant is protected by the etching process of the present invention.

In a third step **14**, the substrate is rinsed in a circulating bath of deionized water. A pair of probes connected to a resistance meter are placed in the bath. As those skilled in the art are aware, pure deionized water has a very low conductivity, i.e., a very high resistivity. If the two probes are placed one centimeter apart, the resistance meter registers approximately 18 mega-ohms (MΩ) for pure deionized water. At the beginning of the rinsing process, the resistance meter registers a resistance value approaching zero because the etchant dissolved in the deionized water has a high electrical conductivity. As the rinsing process continues, the concentration of the etchant dissolved in the deionized water decreases, resulting in a decreased conductivity. The substrate is considered to be sufficiently rinsed when the deionized water in the circulating bath becomes substantially nonconductive. For example, the rinsing process continues until the resistance meter registers a resistance value higher than a predetermined value such as, for example, 10MΩ. It should be noted that the criteria of how long the rinsing process continues is not limited to sensing the conductivity of the deionized water. In another approach, the rinsing process is set to last for a predetermined time period.

In a fourth step **15**, the substrate is submerged in a recirculating bath of hydrogen peroxide solution having a concentration of, for example, 30 percent (%). This step of bathing the substrate in hydrogen peroxide lasts for a time period such as, for example, 15 minutes.

In a fifth step **17**, the substrate is rinsed in a circulating bath of deionized water as in step **14**.

It should be noted that, although preferred in some applications, step **15** and step **17** are optional.

In a sixth step **18**, the substrate is dried in an environment of circulating isopropyl alcohol vapor having a concentration of, for example, 70%, and at a temperature such as, for example, 180° C. The isopropyl alcohol vapor absorbs the moisture on the substrate.

By now it should be appreciated that a method for etching a substrate has been provided. The etching process in accordance with the present invention protects the polycrystalline silicon on the substrate from being etched by displacing the oxygen dissolved in the etchant. The process is simple and easy to implement by injecting an inert gas into the etchant.

What is claimed is:

1. A method for etching a dielectric layer on a semiconductor, comprising the steps of:

providing a semiconductor substrate having the dielectric layer disposed thereon;

providing a purged etchant; and

submerging a portion of the semiconductor substrate in the purged etchant to etch the dielectric layer on the semiconductor substrate.

2. The method for etching a dielectric layer on a semiconductor as claimed in claim **1**, wherein step of providing a purged etchant includes injecting a purgative gas into an etchant to purge the etchant.

3. The method for etching a dielectric layer on a semiconductor as claimed in claim **2**, wherein the step of injecting a purgative gas into an etchant includes injecting a gas selected from the group consisting of nitrogen, carbon dioxide, helium, neon, argon, krypton, and xenon.

4. The method for etching a dielectric layer on a semiconductor as claimed in claim **2**, wherein the step of injecting a purgative gas into an etchant includes the steps of:

generating a recirculating path for the etchant;

installing a filter in the recirculating path; and

injecting the purgative gas into the etchant in a direction opposite to a flow of the etchant while the etchant is flowing through the recirculating path.

5. The method for etching a dielectric layer on a semiconductor as claimed in claim **4**, wherein the step of generating a recirculating path includes the steps of:

providing a tub having a bottom, wherein the bottom has at least one injector;

filling the tub with the etchant, wherein the etchant overflows the tub; and

pumping the etchant overflowing the tub through the recirculating path to the tub via the at least one injector.

6. The method for etching a dielectric layer on a semiconductor as claimed in claim **1**, further comprising the step of dipping the semiconductor substrate in a surfactant before submerging a portion of the semiconductor substrate in the purged etchant.

7. The method for etching a dielectric layer on a semiconductor as claimed in claim **1**, further comprising the steps of:

rinsing the semiconductor substrate after the step of submerging a portion of the semiconductor substrate in the purged etchant; and

drying the semiconductor substrate after the step of rinsing the semiconductor substrate.

8. The method for etching a dielectric layer on a semiconductor as claimed in claim **7**, wherein the step of rinsing the semiconductor substrate includes the steps of:

placing the semiconductor substrate in a circulating bath of deionized water;

sensing a conductivity of the deionized water; and

removing the semiconductor substrate from the circulating bath in response to the circulating bath of deionized water being substantially nonconductive.

9. The method for etching a dielectric layer on a semiconductor as claimed in claim **7**, wherein the step of drying the semiconductor substrate includes placing the semiconductor substrate in an isopropyl alcohol vapor.

10. The method for etching a dielectric layer on a semiconductor as claimed in claim **7**, further comprising the step of bathing the semiconductor substrate in hydrogen peroxide after the step of rinsing the semiconductor substrate and before the step of drying the semiconductor substrate, wherein the step of bathing the semiconductor substrate in hydrogen peroxide includes the steps of:

submerging a portion of the semiconductor substrate in a hydrogen peroxide solution; and

rinsing the semiconductor substrate after the step of submerging a portion of the semiconductor substrate in a hydrogen peroxide solution.

11. A method for etching a dielectric material over a semiconductor material, comprising the steps of:

providing a bath of an etchant;

injecting a purgative gas into the etchant;

submerging a portion of the semiconductor material in the bath;

rinsing the semiconductor material after the step of submerging a portion of the semiconductor material in the bath; and

drying the semiconductor material after the step of rinsing the semiconductor material.

12. The method for etching a dielectric material over a semiconductor material as claimed in claim **11**, wherein the

step of injecting a purgative gas includes injecting a gas selected from the group consisting of nitrogen, carbon dioxide, helium, neon, argon, krypton, and xenon.

13. The method for etching a dielectric material over a semiconductor material as claimed in claim **11**, wherein the step of injecting a purgative gas includes the steps of:

generating a recirculating path for the etchant;

installing a filter in the recirculating path; and

injecting the purgative gas into the etchant in a direction opposite to a flow of the etchant while the etchant is flowing through the recirculating path.

14. The method for etching a dielectric material over a semiconductor material as claimed in claim **11**, further comprising the step of dipping the semiconductor material in a surfactant before submerging a portion of the semiconductor material in the bath.

15. The method for etching a dielectric material over a semiconductor material as claimed in claim **11**, further comprising the step of bathing the semiconductor material in hydrogen peroxide after the step of rinsing the semiconductor material and before the step of drying the semiconductor material, wherein the step of bathing the semiconductor material in hydrogen peroxide includes the steps of:

submerging a portion of the semiconductor material in a hydrogen peroxide solution; and

rinsing the semiconductor material after the step of submerging a portion of the semiconductor material in the hydrogen peroxide solution.

16. A method for etching an oxide layer on a semiconductor wafer, comprising the steps of:

dipping the semiconductor wafer in a surfactant;

injecting a purgative gas into a tub filled with an etchant;

submerging a portion of the semiconductor wafer in the tub;

rinsing the semiconductor wafer after submerging a portion of the semiconductor wafer in the tub; and

drying the semiconductor wafer after rinsing the semiconductor wafer.

17. The method for etching an oxide layer on a semiconductor wafer as claimed in claim **16**, wherein the step of injecting a purgative gas includes injecting a gas selected from the group consisting of nitrogen, carbon dioxide, helium, neon, argon, krypton, and xenon.

18. The method for etching an oxide layer on a semiconductor wafer as claimed in claim **16**, wherein the step of injecting a purgative gas includes the steps of:

generating a recirculating path for the etchant in the tub;

installing a filter in the recirculating path;

pumping a portion of the etchant in the tub through the recirculating path;

injecting the purgative gas into the etchant in a direction opposite to a flow of the etchant while the etchant is flowing through the recirculating path; and

pumping the etchant with the purgative gas in the recirculating path to the tub via at least one injector located at a bottom of the tub.

19. The method for etching an oxide layer on a semiconductor wafer as claimed in claim **16**, further comprising the step of bathing the semiconductor wafer in hydrogen peroxide after the step of rinsing the semiconductor wafer and before the step of drying the semiconductor wafer, wherein the step of bathing the semiconductor wafer in hydrogen peroxide includes the steps of:

submerging a portion of the semiconductor wafer in a hydrogen peroxide solution; and

rinsing the semiconductor wafer after the step of submerging a portion of the semiconductor wafer in the hydrogen peroxide solution.

20. A method for etching a dielectric layer over a semiconductor material, comprising the step of using a degassed etchant solution to etch the dielectric layer.

* * * * *

Exhibit L

US005776798A

United States Patent [19]

Quan et al.

[11] Patent Number: 5,776,798

[45] Date of Patent: Jul. 7, 1998

[54] **SEMICONDUCTOR PACKAGE AND METHOD THEREOF**

[75] Inventors: **Son Ky Quan**, Fountain Hills; **Samuel L. Coffman**, Scottsdale; **Bruce Reid**, Mesa; **Keith E. Nelson**, Tempe, all of Ariz.; **Deborah A. Hagen**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **708,296**

[22] Filed: **Sep. 4, 1996**

[51] **Int. Cl.**[6] **H01L 21/44**

[52] **U.S. Cl.** **438/112**; 438/460

[58] **Field of Search** 438/112, 113, 438/460, 464, 465

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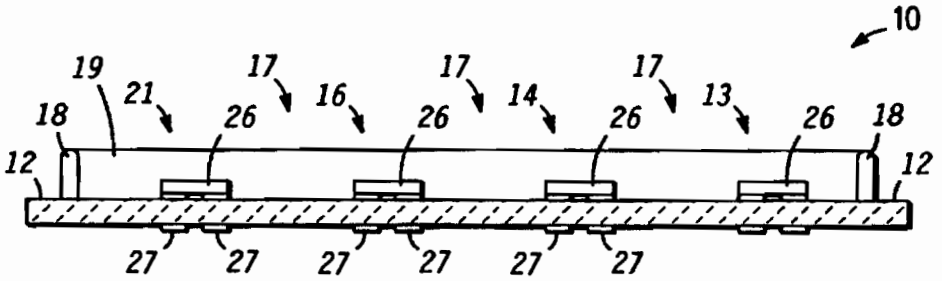
Primary Examiner—Kevin Picardat

Attorney, Agent, or Firm—Robert F. Hightower

[57] **ABSTRACT**

A semiconductor package substrate (**10**) has an array of package sites (**13,14,16,21,22**, and **23**) that are substantially identical. The entire array of package sites (**13,14,16,21,22**, and **23**) is covered by an encapsulant (**19**). The individual package sites (**13,14,16,21,22**, and **23**) are singulated by sawing through the encapsulant (**19**) and the underlying semiconductor package substrate (**10**).

12 Claims, 1 Drawing Sheet



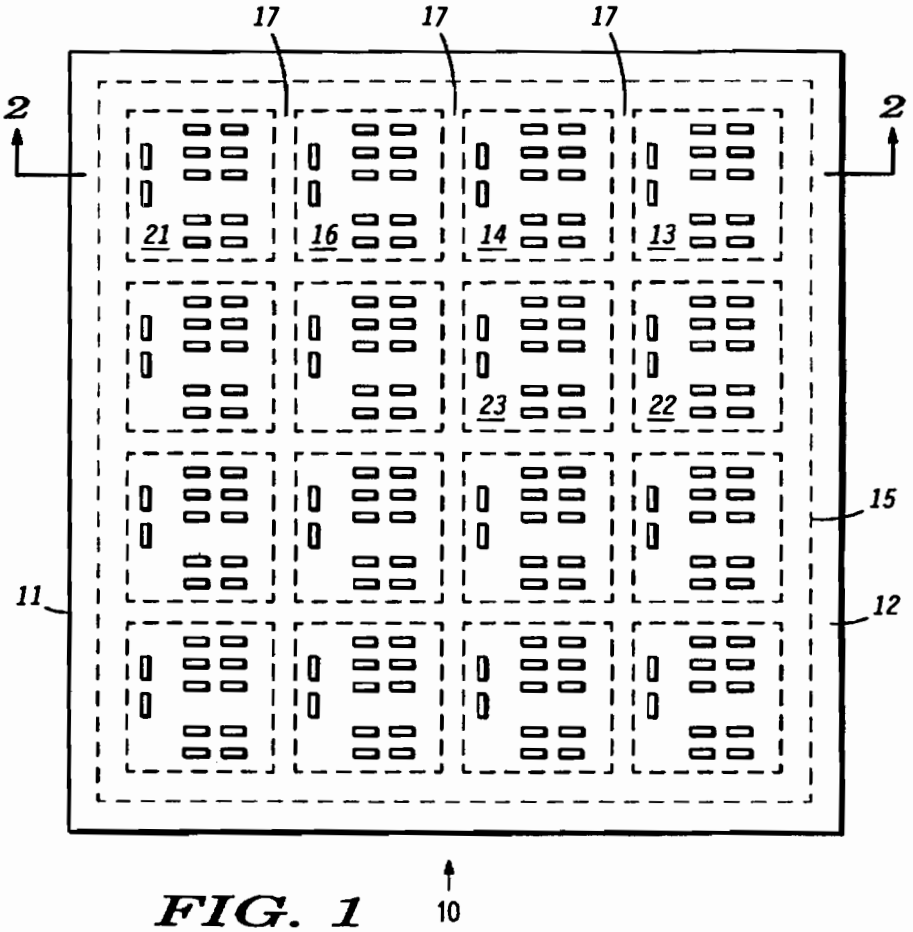


FIG. 1

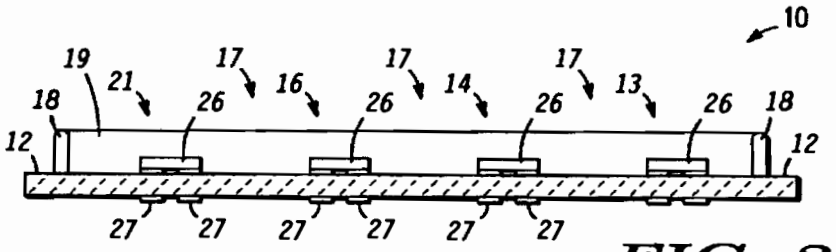


FIG. 2

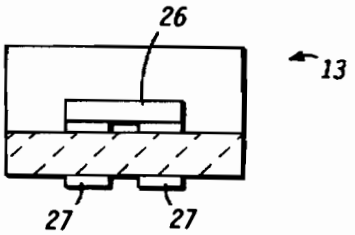


FIG. 3

SEMICONDUCTOR PACKAGE AND METHOD THEREOF

BACKGROUND OF THE INVENTION

The present invention relates, in general, to packaging techniques, and more particularly, to a novel semiconductor package.

In the past, the semiconductor industry has utilized a variety of encapsulation techniques for forming the body of semiconductor packages. Typically, the semiconductor and other devices are assembled onto an interconnect platform or substrate such as a leadframe, printed circuit board or ceramic substrate. One particular encapsulating technique, commonly referred to as glob-top, involves dispensing an encapsulant to cover semiconductor devices or other components that are assembled onto the substrate. One problem with this prior technique is the planarity of the top surface of the encapsulant. Often, the top surface has a convex shape. Because of the convex shape, automated pick and place equipment can not utilize the resulting semiconductor package. Also, it is difficult to mark the top surface because of the convex shape.

Such techniques usually encapsulate a single assembly site on a substrate and after encapsulation, the assembly site is singulated to form an individual package. Consequently, assembly time and singulation time are long and result in high package cost.

Accordingly, it is desirable to have a semiconductor package that has a substantially planar surface that can be utilized with automated pick and place equipment, that is easily marked, and that increases throughput thereby reducing the cycle time and assembly costs.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a plan view of a semiconductor package at a stage of manufacturing in accordance with the present invention;

FIG. 2 illustrates a cross-sectional view of the package of FIG. 1 at a subsequent manufacturing stage; and

FIG. 3 illustrates a cross-sectional view of a singulated semiconductor package in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates an embodiment of a semiconductor package substrate or semiconductor package 10 at a stage of manufacturing. Package 10 includes an interconnect substrate 11 that has a plurality of package sites such as package sites 13, 14, 16, 21, 22, and 23. As will be seen hereinafter, each of sites 13, 14, 16, 21, 22, and 23 will subsequently be singulated into an individual singulated semiconductor package. Each of sites 13, 14, 16, 21, 22, and 23 are substantially identical and have areas within each site for attaching and interconnecting a plurality of electronic components such as active semiconductor devices, and passive elements such as resistors and capacitors. Each of sites 13, 14, 16, 21, 22, and 23 are separated by a space, for example space 17 between sites 16 and 21, so that each site may be singulated into an individual package.

Substrate 11 can have a variety of forms including a stamped leadframe, a ceramic substrate, a printed circuit board substrate, and other configurations that are well known to those skilled in the art. As shown in FIG. 1, substrate 11 is a ceramic substrate having multiple layers of electrical interconnect separated by dielectrics, and multiple attachment areas.

Substrate 11 also includes a dam-bar area 12 around the periphery of substrate 11, thus, surrounding the periphery of the plurality of package sites as indicated by a dashed line 15. As will be seen hereinafter, dam-bar area 12 is used for encapsulating package 10 and individual packages formed by each package site of the plurality of package sites, such as sites 13, 14, 16, 21, 22, and 23.

FIG. 2 illustrates a cross-sectional schematic of package 10 at a subsequent stage of manufacturing and is taken along cross-sectional line 2—2 shown in FIG. 1. The same reference numbers are used to represent the same elements among the drawings. Typically, components such as semiconductor devices or passive elements are attached to each package site as illustrated by a component 26 attached to sites 13, 14, 16, and 21. Many components may be attached to each package site, device 26 is shown only for illustration purposes. As shown in FIG. 2, encapsulating each package site of the plurality of package sites and associated components includes forming a dam-bar 18 on area 12. Dam-bar 18 creates a cavity containing the plurality of package sites. Dam-bar 18 is formed by dispensing a first encapsulating material onto area 12. The first encapsulating material has a first viscosity that is sufficiently high so that the encapsulating material does not flow across substrate 11 but substantially remains as dispensed onto area 12. Typically, the first encapsulating material has a high viscosity that is greater than approximately 500,000 centi-poise (cps), and typically has a viscosity of 1,000,000 to 2,000,000 cps at approximately 25° C. (degrees Celsius). One suitable first encapsulating material for dam-bar 18 is a rigid thermosetting epoxy such as FP-4451 manufactured by Hysol-Dexter of Industry, Calif.

Generally, the first encapsulating material is heated during dispensing by heating the syringe or dispensing mechanism so that the first encapsulating material can be dispensed. Additionally, substrate 11 generally is also heated to a higher temperature so that the first encapsulating material flows sufficiently to form dam-bar 18. Generally, the dispensing mechanism or syringe is heated to approximately forty to fifty degrees Celsius (40°–50° C.), and substrate 11 generally is heated to approximately eighty to ninety degrees Celsius.

Thereafter, a second encapsulating material is dispensed within the cavity formed by dam-bar 18 to form an encapsulant 19 covering the components on substrate 11. The thickness of encapsulant 19 is sufficient to cover and protect components such as component 26 formed on substrate 11. The second encapsulating material has a second viscosity that is sufficiently low so that the second encapsulating material flows to fill the cavity leaving no voids and surrounds the components and attachment wires used to connect components to substrate 11. The second viscosity is less than the 500,000 cps high viscosity of the first encapsulating material and typically is approximately 20,000 to 200,000 cps at 25° C. One example of a suitable material for the second encapsulating material is FP-4650 manufactured by Hysol-Dexter. Additionally, the second encapsulating material typically has the same chemical base as the first encapsulating material so that the two materials bond at the interface to minimize separation and potential contamination. During dispensing, the second encapsulating material and substrate 11 are heated similarly to the heating used for dispensing the first encapsulating material.

After dispensing, the first and second encapsulating material are heated to gel both encapsulating materials in order to control subsequent out gassing and warpage of substrate 11. Typically, both encapsulating materials are gelled for

approximately one hour at one hundred ten degrees Celsius. Subsequently, dam-bar **18** and encapsulant **19** are cured so that encapsulant **19** forms a continuous encapsulating material covering the underlying components. Typically the curing is performed at a temperature of approximately 165° C. for a time of up to two hours. After curing, each individual package site is singulated into a singulated package by using space **17** for sawing completely through encapsulant **19** and substrate **11**. For example, a ceramic saw is used to saw through encapsulant **19** and substrate **11** when substrate **11** is ceramic material. Other singulation techniques could be utilized including laser cutting through encapsulant **19** and substrate **11**.

The area covered by encapsulant **19** should be larger than the meniscus formed by the second encapsulating material so that the top surface of encapsulant **19** remains substantially planar. For example, the top surface should have a deviation of less than plus or minus 0.13 millimeters across the surface of encapsulant **19**. As shown in FIG. **2**, the plurality of package sites are formed in an 4×4 array but could also be formed in other arrays. An array that is sixty by sixty millimeters provides a sufficient area to provide the desired planarity.

It should be noted that other encapsulating techniques could be utilized to cover the plurality of package sites with an encapsulating material in order to encapsulate package **10**. For example, dam-bar **18** could be a premanufactured frame applied to area **12**, and overmolding or other techniques could be used for the encapsulating. Thereafter each package site can be singulated as described hereinbefore.

FIG. **3** illustrates a cross-sectional view of a singulated package formed from a package site such as package site **13** shown in FIG. **1** and FIG. **2**.

By now it should be appreciated that there has been provided a novel semiconductor package and method therefor. Forming a plurality of package sites on a substrate and using one dam-bar around the entire periphery surrounding the plurality of package sites, facilitates forming a substantially planar surface on the encapsulant. Forming a substantially planar surface allows each singulated package to have a substantially planar surface and facilitates utilization with automated pick and place equipment, and also facilitates clear marking of each singulated package. Forming the plurality of package sites adjacent to each other and covering the plurality of package sites with one continuous encapsulant minimizes space required to singulate the package sites and maximizes the number of package sites on a substrate thereby providing the smallest package outline and lowering package costs.

We claim:

1. A method of forming a semiconductor package comprising:

forming a substrate having a plurality of package sites and an electronic component attached to the plurality of package sites;

encapsulating the plurality of package sites wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites; and

singulating through the encapsulating material to singulate each package site into an individual package.

2. A method of forming a semiconductor package comprising:

encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming the encapsulating material to have a top surface planarity deviation of less than 0.13 millimeters; and

singulate through the encapsulating material to singulate each package site.

3. A method of forming a semiconductor package comprising:

encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming a dam bar surrounding the periphery of the plurality of package sites for forming a cavity containing the plurality of package sites, and dispensing the encapsulating material within the cavity; and

singulating through the encapsulating material to singulate each package site.

4. The method of claim **3** wherein forming the dam bar includes dispensing a first encapsulating material having a first viscosity.

5. The method of claim **4** wherein dispensing the encapsulating material within the cavity includes dispensing a second encapsulating material having a second viscosity that is lower than the first viscosity.

6. The method of claim **5** wherein dispensing the first encapsulating material having the first viscosity includes having a viscosity of 1,000,000 to 2,000,000 cps.

7. The method of claim **5** wherein dispensing the second encapsulating material having the second viscosity includes having a viscosity less than 500,000 cps.

8. The method of claim **5** further including gelling both the first and second encapsulating materials prior to curing both the first and second encapsulating materials.

9. The method of claim **5** wherein dispensing the first encapsulating material includes heating the first encapsulating material.

10. The method of claim **5** wherein dispensing the second encapsulating material includes heating the second encapsulating material.

11. The method of claim **1** wherein singulating through the encapsulating material includes sawing through the encapsulating material and the substrate.

12. The method of claim **1** wherein encapsulating the plurality of package sites includes encapsulating by overmolding.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,776,798
DATED : July 7, 1998
INVENTOR(S) : Son Quan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, claim 2, line 13, delete "singulate" and insert –singulating--.

Signed and Sealed this

Fifteenth Day of June, 1999

Attest:

Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks

Exhibit M

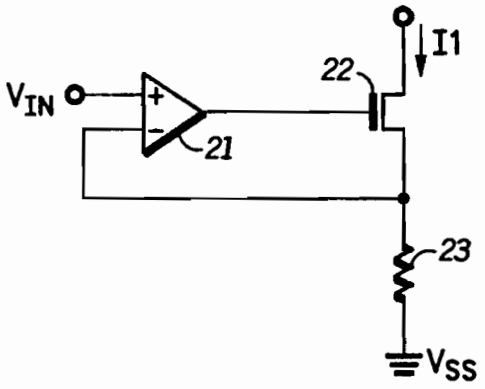


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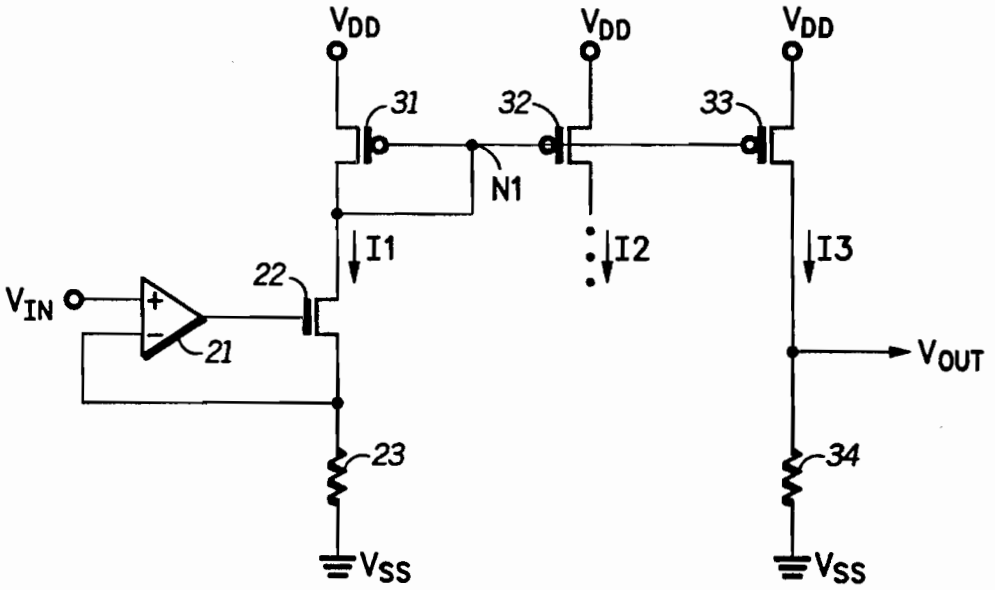
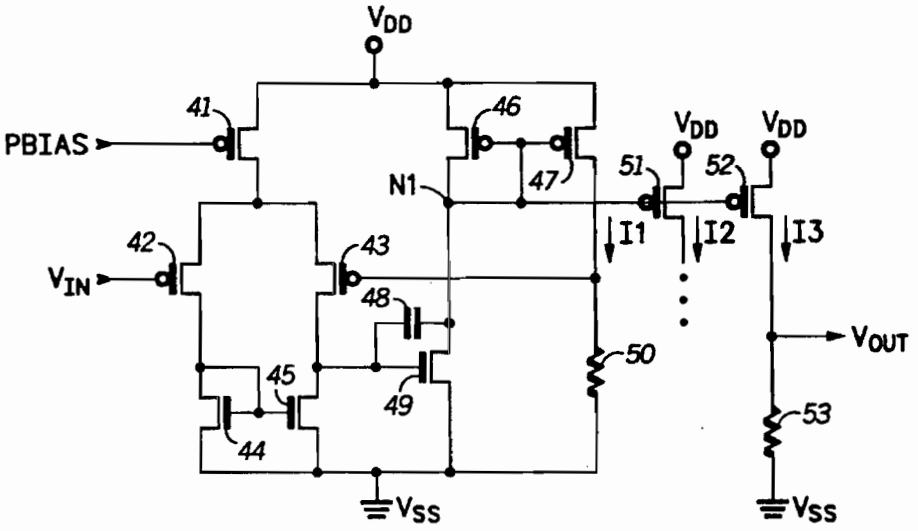
FIG.1
-PRIOR ART-



30

FIG.2
-PRIOR ART-



40

FIG. 3

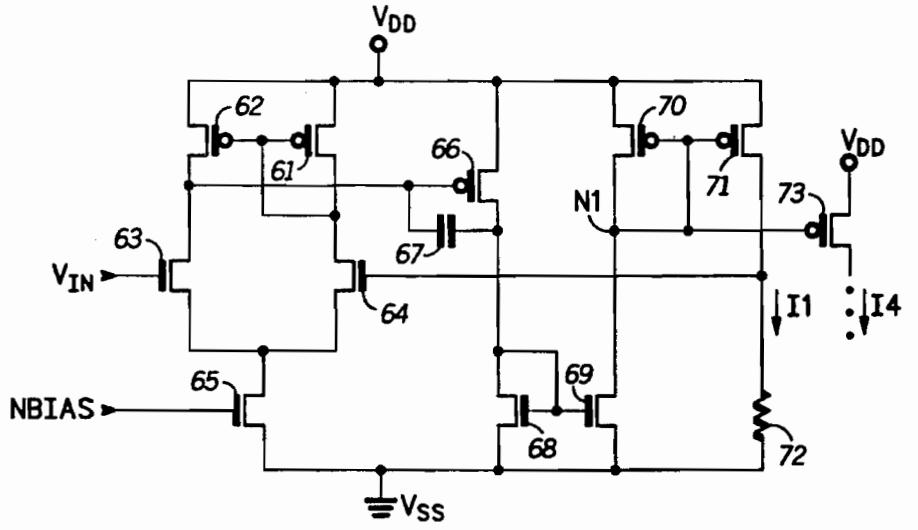


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FIG. 4

LOW-VOLTAGE PRECISION CURRENT GENERATOR

FIELD OF THE INVENTION

This invention relates generally to analog circuits, and more particularly, to low-voltage precision current generators.

BACKGROUND OF THE INVENTION

Current generators (commonly referred to as current sources and current sinks) are important elements in the design of many electrical circuits. For example, current generators are used in differential amplifiers. Input voltages received at control electrodes of respective input transistors selectively divert the current provided by the current generator to change the output voltage of the amplifier. In many analog circuits, it is further necessary to provide a current whose magnitude is proportional to a reference voltage. For example, a voltage controlled oscillator often employs a voltage controlled current source. In commercial integrated circuits, it is desirable for the voltage-controlled current source to function under a variety of conditions, including variations in power supply voltage, temperature, and manufacturing process variations in which transistor thresholds vary. Some integrated circuits, once required to operate with a five-volt power supply voltage, must now function at a lower power supply voltage such as three volts. Thus, precision current generators are needed for low voltage operation.

SUMMARY OF THE INVENTION

Accordingly, there is provided, in one form, a low voltage precision current generator coupled to first and second power supply voltage terminals comprising an amplifier, a first transistor, a current portion, and an output portion. The amplifier provides a first voltage signal in response to a difference in voltage between first and second input signals respectively received at first and second input terminals thereof. The first transistor has a first current electrode, a control electrode for receiving the first voltage signal, and a second current electrode coupled to the second power supply voltage terminal. The current portion is coupled to the second input terminal of the amplifier and to the first current electrode of the first transistor, and provides a reference current proportional to a difference in voltage between the second input terminal of the amplifier and a predetermined voltage terminal. The output portion is coupled to the current portion and provides the precision current in response to the reference current.

These and other features and advantages will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates in partial schematic and partial block form a voltage-controlled current generator circuit known in the prior art.

FIG. 2 illustrates in partial schematic and partial block form a voltage-controlled current generator circuit known in the prior art and adapted from the voltage-controlled current generator circuit of FIG. 1.

FIG. 3 illustrates in schematic form a low-voltage precision current generator circuit in accordance with the present invention.

FIG. 4 illustrates in schematic form an alternate embodiment of the low-voltage precision current generator circuit of FIG. 3 in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates in partial schematic and partial block from a voltage-controlled current generator circuit 20 known in the prior art. See Gregorian, R. and Temes, G. C., *Analog MOS Integrated Circuits for Signal Processors*, John Wiley & Sons, New York, 1986, p. 450. Circuit 20 includes an operational amplifier 21, an N-channel transistor 22, and a resistor 23. Operational amplifier 21 has a positive input terminal for receiving an input voltage labelled "V_{IN}", a negative input terminal, and an output terminal. Transistor 22 has a drain for receiving a current labelled "I1", a gate connected to the output terminal of operational amplifier 21, and a source connected to the negative input terminal of operational amplifier 21. Resistor 23 has a first terminal connected to the source of transistor 22 and to the negative input terminal of operational amplifier 21, and a second terminal connected to a power supply voltage terminal labelled "V_{SS}". V_{SS} is a more-negative power supply voltage terminal typically at 0 volts. An additional, more-positive power supply voltage terminal labelled "V_{DD}" is not shown in FIG. 1.

Analysis of the operation of circuit 20 is straightforward. Operational amplifier 21 changes the voltage at its output terminal until the voltage at the negative input terminal equals the voltage at the positive input terminal. Thus, the voltage at the first terminal of resistor of resistor 23 is equal to V_{IN}. The current flowing through resistor 23, and thus through the drain-to-source path of transistor 22, is provided by

$$I1 = V_{IN}/R_{IN} \quad (1)$$

where R_{IN} is the resistance of resistor 23. Thus output current I1 is proportional to the input voltage V_{IN}.

Circuit 20 of FIG. 1 forms a current sink, causing current I1 to flow from the drain of transistor 21 into the more-negative power supply voltage terminal V_{SS}. However, a modification of circuit 20 of FIG. 1 provides a voltage controlled current source. FIG. 2 illustrates in partial schematic and partial block form a voltage-controlled current generator circuit 30 known in the prior art and adapted from voltage-controlled current generator circuit 20 of FIG. 1. Circuit 30 has elements corresponding to operational amplifier 21, transistor 22, and resistor 23 and those elements are similarly numbered in FIG. 2. Circuit 30 additionally includes P-channel transistors 31-33, and resistor 34. Transistor 31 has a source connected to V_{DD}, a gate, and a drain connected to the gate of transistor 31 at a node labelled "N1", and to the drain of transistor 22. Transistor 32 has a source connected to V_{DD}, a gate connected to node N1, and a drain for providing a current labelled "I2". Transistor 33 has a source connected to V_{DD}, a gate connected to node N1, and a drain for providing a current labelled "I3" at a node providing a voltage labelled "V_{OUT}". Resistor 34 has a first terminal connected to the drain of transistor 33, and a second terminal connected to V_{SS}.

Circuit **30** illustrates the uses to which circuit **20** of FIG. **1** may be put. First, transistor **31** mirrors current I1 through transistor **32** to provide current I2 flowing from the drain electrode thereof to elements not shown in FIG. **2**. Thus, circuit **30** functions as a current source. I1 is further mirrored through transistor **33** to provide a current I3. Resistor **34** converts the current flowing through transistor **33** and resistor **34** into voltage V_{OUT}. The magnitude of V_{OUT} can also be easily determined. The current flowing through the drain-to-source path of transistor **22**, I1, is mirrored through transistor **33**. If the transistor gate sizes are equal, measured in the gate width-to-length (W/L) ratio, then I3=I1. If the resistance of resistor **34** is labelled "R_{OUT}", then

$$V_{OUT}=I3*R_{OUT}=V_{IN}(R_{OUT}/R_{IN}) \quad (2)$$

Further, assume that the actual width-to-length ratio of transistor **31** is equal to $(W/L)_1$. If the actual width-to-length ratio of transistor **32** is equal to $X*(W/L)_1$, then

$$I2=X*I1 \quad (3)$$

Thus, when a current mirror is used as shown in FIG. **2**, a voltage-controlled current source is produced and the current provided by the current source may be modified.

However, circuit **30** has a problem at low power supply voltage. The headroom requirements of transistors **31** and **22** limit the operation of circuit **30** at low power supply voltages. Since operational amplifier **21** sets the voltage at the source of transistor **22** to be equal to V_{IN}, the drain-to-source voltage (V_{DS}) of transistor **31** plus the V_{DS} of transistor **22** must equal ($V_{DD}-V_{IN}$). V_{IN} is typically a bandgap reference voltage with a value of about 1.2 volts. Thus, at a desired power supply voltage of 3 volts, the sum of the V_{DS} of transistors **31** and **22** must equal 1.8 volts. Transistor **31** is diode-connected; thus, its V_{DS} equals its gate-to-source voltage (V_{GS}). In order to keep current I1 flowing, the V_{GS}, and hence the V_{DS} of transistor **31** must remain constant. As V_{DD} drops, the V_{DS} of transistor **31** is still maintained. At the same time, the voltage at the drain of transistor **22** drops while the voltage at the source of transistor **22** remains constant. Thus, as V_{DD} drops, the V_{DS} of transistor **22** drops, eventually taking transistor **22** out of saturation. As soon as transistor **22** comes out of saturation, the precision current reference is lost. For practical purposes, and for typical reference currents, circuit **30** is limited in operation to a value of V_{DD} of about 4 volts or greater.

FIG. **3** illustrates in schematic form a low-voltage precision current generator circuit **40** in accordance with the present invention. Circuit **40** includes P-channel transistors **41–43**, N-channel transistors **44** and **45**, P-channel transistors **46** and **47**, a capacitor **48**, an N-channel transistor **49**, a resistor **50**, P-channel transistors **51** and **52**, and a resistor **53**. For circuit **40**, V_{DD} provides a first power supply voltage terminal and V_{SS} provides a second power supply voltage terminal. Transistor **41** has a source connected to V_{DD}, a gate for receiving a reference voltage labelled "PBIAS", and a drain. Transistor **42** has a source connected to the drain of transistor **42**, a gate for receiving reference voltage V_{IN}, and a drain. In the illustrated embodiment V_{IN} is a bandgap reference voltage equal to approximately 1.2 volts; however, in other embodiments, V_{IN} can be a variable voltage. Transistor **43** has a source connected to the drain of transistor **41**, a gate, and a drain. Transistor **44** has a drain connected to the drain of transistor **42**, a gate connected to the drain of transistor **42**, and a source connected to V_{SS}. Transistor **45** has a drain connected to the drain of transistor **43**, a gate connected to the drain of transistor **42**, and a source connected to V_{SS}. Transistor **46** has a source connected to V_{DD}, a gate, and a drain connected to the gate of transistor **46**. Transistor **47** has a source connected to V_{DD}, a gate connected to the drain of transistor **46**, and a drain connected to the gate of transistor **43** and also providing current I1. Capacitor **48** has a first terminal connected to the drain of transistor **43**, and a second terminal connected to the drain of transistor **46**. Transistor **49** has a drain connected to the drain of transistor **46**, a gate connected to the drain of transistor **43**, and a source connected to V_{SS}. Resistor **50** has a first terminal connected to the drain of transistor **47**, and a second terminal connected to V_{SS}. Transistor **51** has a source connected to V_{DD}, a gate connected to the drain of transistor **46**, and a drain for providing current I2. Transistor **52** has a source connected to V_{DD}, a gate connected to the drain of transistor **46**, and a drain for providing current I3 to the node providing V_{OUT}. Resistor **53** has a first terminal connected to the drain of transistor **52**, and a second terminal connected to V_{SS}.

The general operation of circuit **40** is easily analyzed. Transistors **41–45** function as an differential amplifier, with the gate of transistor **42** functioning as the positive input terminal, the gate of transistor **43** functioning as the negative input terminal, and the drain of transistor **43** functioning as the output terminal. Transistor **46** will source whatever current is required to make transistor **47** mirror a current determined as

$$I1=V_{IN}/R_{IN} \quad (4)$$

where R_{IN} is the resistance of resistor **50**. If transistors **46** and **47** have the same W/L ratios, then the currents conducted through transistors **46** and **47** will be the same and equal to I1. Thus, the voltage at the drain of transistor **43** changes until the voltage at the gate of transistor **43** is equal to V_{IN}. The voltage at the first terminal of resistor **50** is set to V_{IN}, and current I1 (similarly labelled as in FIGS. **1** and **2**) flows through resistor **50**. The current I1 provided by circuit **40** is identical to current I1 provided by circuit **30**, as illustrated by comparing equation (4) to equation (1). In order for I1 to flow through resistor **50**, I1 must flow through the drain-to-source paths of transistors **46** and **47** in order to be mirrored by transistor **46** through transistor **47**. Thus, the voltage at node N1 is set to bias a transistor of a given W/L ratio to conduct current I1. As before, transistor **51** may have a different W/L ratio which is a multiple or fraction of the W/L ratio of transistor **46** such that a different current I2 is provided to circuitry not shown in FIG. **3**. Furthermore, transistor **52** may have the same W/L ratio as transistor **46** to provide I3=I1 from the drain of transistor **52**. Resistor **53** converts I3 into voltage V_{OUT} as follows:

$$V_{OUT}=I3*R_{OUT}=V_{IN}(R_{OUT}/R_{IN}) \quad (5)$$

where R_{OUT} is equal to the resistance of resistor **53**. Thus, circuit **40** performs an identical operation as circuit **30** of FIG. **2**, as illustrated by comparing equation (5) to equation (2).

At the same time, circuit 40 solves the headroom problem associated with circuit 30 of FIG. 2 to guarantee operation at substantially lower power supply voltage, in the illustrated embodiment of V_{DD} below 3 volts. As V_{DD} drops, the available headroom is $(V_{DD}-V_{IN})$, which is equal to about 1.8 volts. However, only a single transistor, transistor 47, must remain in saturation within the bounds of this headroom. Under typical MOS geometries, 1.8 volts is substantially greater than the V_{DS} of P-channel MOS transistor 47 which occurs when transistor 46 is conducting current I1. Thus, transistor 47 remains saturated at power supply voltages of 3.0 volts and below. Capacitor 48 is included to provide dominant pole compensation. As the number of transistors to which node N1 is connected increases, the capacitance at the drain of transistor 46 increases. Capacitor 48 is included to ensure that the drain of transistor 43 remains the dominant pole. Thus, stability is ensured.

FIG. 4 illustrates in schematic form an alternate embodiment 60 of low-voltage precision current generator circuit 40 of FIG. 3 in accordance with the present invention. It should be apparent however that circuit 60 is not a complete mirror image of circuit 40 for the reasons set forth in more detail below. Circuit 60 includes P-channel transistors 61 and 62, N-channel transistors 63-65, a P-channel transistor 66, a capacitor 67, N-channel transistors 68 and 69, P-channel transistors 70 and 71, a resistor 72, and a P-channel transistor 73. For circuit 60, V_{SS} provides a first power supply voltage terminal and V_{DD} provides a second power supply voltage terminal. Transistor 61 has a source connected to V_{DD}, a gate, and a drain connected to the gate of transistor 61. Transistor 62 has a source connected to V_{DD}, a gate connected to the drain of transistor 61, and a drain. Transistor 63 has a drain connected to the drain of transistor 62, a gate for receiving signal V_{IN}, and a source. Transistor 64 has a drain connected to the drain of transistor 61, a gate, and a source connected to the source of transistor 63. Transistor 65 has a drain connected to the drains of transistors 63 and 64, a gate for receiving a bias signal labelled "NBIAS", and a source connected to V_{SS}. NBIAS is a voltage which biases transistor 65 to act as a current source. Transistor 66 has a source connected to V_{DD}, a gate connected to the source of transistor 62, and a drain. Capacitor 67 has a first terminal connected to the drain of transistor 62, and a second terminal connected to the drain of transistor 66. Transistor 68 has a drain connected to the drain of transistor 66, a gate connected to the drain of transistor 68, and a source connected to V_{SS}. Transistor 69 has a drain, a gate connected to the drain of transistor 66, and a source connected to V_{SS}. Transistor 70 has a source connected to V_{DD}, a gate, and a drain connected to the gate of transistor 70 and to the drain of transistor 69 at node N1. Transistor 71 has a source connected to V_{DD}, a gate connected to the drain of transistor 70, and a drain providing current I1. Resistor 72 has a first terminal connected to the drain of transistor 71 and the gate of transistor 64, and a second terminal connected to V_{SS}. Transistor 73 has a source connected to V_{DD}, a gate connected to the drain of transistor 70, and a source for providing a current labelled "I4" provided to circuitry not shown in FIG. 4.

Circuit 60 functions as the complementary analog of circuit 40 of FIG. 3. It should be recognized that first power supply voltage terminal V_{DD} in circuit 40 corresponds to first power supply voltage terminal V_{SS} in complementary circuit 60, and second power supply voltage terminal V_{SS} in circuit 40 corresponds to second power supply voltage terminal V_{DD} in complementary circuit 60. While it should be readily apparent that circuit 60 has the same advantages as circuit 40 of FIG. 3, an important difference should be noted. While the drain of transistor 49 is connected directly to a current portion formed by transistors 46 and 47 and resistor 50 in circuit 40, the drain of analogous transistor 66 is coupled through a current mirror formed by transistors 68 and 69 to a current portion formed by transistors 70 and 71 and resistor 72 in circuit 60. Also the current mirror in circuits 40 and 60 are similarly formed, with transistor 46 corresponding to transistor 70, transistor 47 to transistor 71, and resistor 50 to resistor 72.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. For example, the same current mirroring technique applied to circuit 60 of FIG. 4 could be applied to circuit 40 of FIG. 3 to provide a voltage-controlled current sink. Circuit 60 could provide a current sink by applying the voltage at the drain of transistor 68 to the gate of an N-channel transistor. In addition, the second terminal of resistor 50 in circuit 40 or resistor 72 in circuit 60 could be coupled to another fixed voltage terminal to still provide a precision reference current. Thus, the present invention encompasses different transistor conductivity types. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

I claim:

1. A low voltage precision current generator coupled to first and second power supply voltage terminals, comprising:

amplifier means for providing a first voltage signal in response to a difference in voltage between first and second input signals respectively received at first and second input terminals thereof;

a first transistor having a first current electrode, a control electrode for receiving said first voltage signal, and a second current electrode coupled to the second power supply voltage terminal;

current means coupled to said second input terminal of said amplifier means and to said first current electrode of said first transistor, for providing a reference current proportional to a difference in voltage between said second input terminal of said amplifier means and a predetermined voltage terminal; and

output means coupled to said current means for providing the precision current in response to said reference current.

2. The low voltage precision current generator of claim 1 wherein said current means comprises:

a second transistor having a first current electrode coupled to the first power supply voltage terminal, a control electrode coupled to said first current electrode of said first transistor, and a second current electrode coupled to said first current electrode of said first transistor;

a third transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode coupled to said first current electrode of said first transistor, and a second current electrode coupled to said second input terminal of

said amplifier means and providing said reference current; and

a resistor having a first terminal coupled to said second current electrode of said third transistor, and a second terminal coupled to said second power supply voltage terminal.

3. The low voltage precision current generator of claim 2 wherein said amplifier means comprises:

a fourth transistor having a first current electrode coupled to the first power supply voltage terminal, a control electrode for receiving a bias signal, and a second current electrode;

a fifth transistor having a first current electrode coupled to said second current electrode of said fourth transistor, a control electrode for providing said first input terminal of said amplifier means, and a second current electrode;

a sixth transistor having a first current electrode coupled to said second current electrode of said fifth transistor, a control electrode coupled to said second current electrode of said fifth transistor, and a second current electrode coupled to the second power supply voltage terminal;

a seventh transistor having a first current electrode coupled to said second current electrode of said fourth transistor, a control electrode for providing said second input terminal of said amplifier means, and a second current electrode; and

an eighth transistor having a first current electrode coupled to said second current electrode of said seventh transistor, a control electrode coupled to said second current electrode of said fifth transistor, and a second current electrode coupled to the second power supply voltage terminal.

4. The low voltage precision current generator of claim 3 further comprising a capacitor having a first terminal connected to said second current electrode of said seventh transistor, and a second terminal coupled to said first current electrode of said first transistor.

5. The low voltage precision current generator of claim 1 wherein said current means is coupled to said first current electrode of said first transistor through a current mirror.

6. The low voltage precision current generator of claim 5 wherein said current mirror comprises:

a second transistor having a first current electrode coupled to the first power supply voltage terminal, a control electrode coupled to said first current electrode of said first transistor, and a second current electrode coupled to said first current electrode of said first transistor; and

a third transistor having a first current electrode coupled to said to first power supply voltage terminal, a control electrode coupled to said first current electrode of said first transistor, and a second current electrode coupled to said current means.

7. The low voltage precision current generator of claim 6 wherein said current means comprises:

a fourth transistor having a first current electrode coupled to said second current electrode of said third transistor, a control electrode coupled to said second current electrode of said third transistor, and a second current electrode coupled tp the second power supply voltage terminal;

a fifth transistor having a first current electrode coupled to said second input terminal of said amplifier means and providing said reference current, a control electrode coupled to said second current electrode of said third transistor, and a second current electrode coupled to the second power supply voltage terminal; and

a resistor having a first terminal coupled to the first power supply voltage terminal, and a second terminal coupled to said first current electrode of said fifth transistor.

8. The low voltage precision current generator of claim 7 wherein said amplifier means comprises:

a sixth transistor having a first current electrode coupled to the first power supply voltage terminal, a control electrode for receiving a bias signal, and a second current electrode;

a seventh transistor having a first current electrode coupled to said second current electrode of said sixth transistor, a control electrode for providing said first input terminal of said amplifier means, and a second current electrode of providing said first voltage signal;

an eighth transistor having a first current electrode coupled to said second current electrode of said seventh transistor, a control electrode, and a second current electrode coupled to the second power supply voltage terminal;

a ninth transistor having a first current electrode coupled to said second current electrode of said sixth transistor, a control electrode for providing said second input terminal of said amplifier means, and a second current electrode; and

a tenth transistor having a first current electrode coupled to said second current electrode of said ninth transistor, a control electrode coupled to said second current electrode of said ninth transistor and to said control electrode of said eighth transistor, and a second current electrode coupled to the second power supply voltage terminal.

9. The low voltage precision current generator of claim 8 further comprising a capacitor having a first terminal connected to said second current electrode of said seventh transistor, and a second terminal coupled to said first current electrode of said first transistor.

10. A low voltage precision current generator comprising:

amplifier means for providing a first voltage signal in response to a difference in voltage between first and second input signals respectively received at first and second input terminals thereof;

a first transistor having a first current electrode coupled to a first power supply voltage terminal, a control electrode, and a second current electrode coupled to said control electrode of said first transistor and providing an second voltage signal thereon;

a second transistor having a first current electrode coupled to said second current electrode of said first transistor, a control electrode for receiving said first voltage signal, and a second current electrode coupled to a second power supply voltage terminal;

a third transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode coupled to said second current electrode of said first transistor, and a second current electrode coupled to said second input terminal of said amplifier means; and

a resistor having a first terminal coupled to said second terminal of said third transistor, and a second

terminal coupled to said second power supply voltage terminal.

11. The low voltage precision current generator of claim 10 further comprising a fourth transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode for receiving said second voltage signal, and a second current electrode for providing the precision current.

12. The low voltage precision current generator of claim 10 further comprising a capacitor having a first terminal coupled to said control electrode of said second transistor, and a second terminal coupled to said second current electrode of said first transistor.

13. The low voltage precision current generator of claim 10 wherein said amplifier means comprises:

a fourth transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode for receiving a bias signal, and a second current electrode;

a fifth transistor having a first current electrode coupled to said second current electrode of said fourth transistor, a control electrode for providing said first input terminal of said amplifier means, and a second current electrode;

a sixth transistor having a first current electrode coupled to said second current electrode of said fifth transistor, a control electrode coupled to said second current electrode of said fifth transistor, and a second current electrode coupled to said second power supply voltage terminal;

a seventh transistor having a first current electrode coupled to said second current electrode of said fourth transistor, a control electrode for providing said second input terminal of said amplifier means, and a second current electrode for providing said first voltage signal; and

an eighth transistor having a first current electrode coupled to said second current electrode of said seventh transistor, a control electrode coupled to said second current electrode of said fifth transistor, and a second current electrode coupled to said second power supply voltage terminal.

14. A low voltage precision current generator comprising:

a first transistor having a first current electrode coupled to a first power supply voltage terminal, a control electrode for receiving a bias signal, and a second current electrode;

a second transistor having a first current electrode coupled to said second current electrode of said first transistor, a control electrode for receiving a first input signal, and a second current electrode;

a third transistor having a first current electrode coupled to said second current electrode of said second transistor, a control electrode coupled to said second current electrode of said second transistor, and a second current electrode coupled to a second power supply voltage terminal;

a fourth transistor having a first current electrode coupled to said second current electrode of said first transistor, a control electrode, and a second current electrode;

an fifth transistor having a first current electrode coupled to said second current electrode of said fourth transistor, a control electrode coupled to said second current electrode of said second transistor, and a second current electrode coupled to said second power supply voltage terminal;

a sixth transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode, and a second current electrode coupled to said control electrode of said sixth transistor and providing an output voltage signal thereon;

a seventh transistor having a first current electrode coupled to said second current electrode of said sixth transistor, a control electrode coupled to said second current electrode of said fourth transistor, and a second current electrode coupled to said second power supply voltage terminal.

an eighth transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode coupled to said second current electrode of said sixth transistor, and a second current electrode coupled to said control electrode of said fourth transistor; and

a resistor having a first terminal coupled to said second terminal of said eighth transistor, and a second terminal coupled to said second power supply voltage terminal.

15. The low voltage precision current generator of claim 14 further comprising a ninth transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode for receiving said second voltage signal, and a second current electrode for providing the precision current.

16. The low voltage precision current generator of claim 14 further comprising a capacitor having a first terminal coupled to said second current electrode of said fourth transistor, and a second terminal coupled to said second current electrode of said sixth transistor.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,124,632

DATED : June 23, 1992

INVENTOR(S) : Carlos A. Greaves

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7, line 63, change "tp", to --to--.
Column 8, line 18, change "of", to --for--.
Column 10, line 30, change ".", to --;--.

Signed and Sealed this

Twenty-eighth Day of September, 1993

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

Exhibit N

US005861347A

United States Patent [19]

Maiti et al.

[11] Patent Number: 5,861,347

[45] Date of Patent: Jan. 19, 1999

[54] **METHOD FOR FORMING A HIGH VOLTAGE GATE DIELECTRIC FOR USE IN INTEGRATED CIRCUIT**

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[73] Assignee: **Motorola Inc.**, Austin, Tex.

[21] Appl. No.: **887,692**

[22] Filed: **Jul. 3, 1997**

[51] **Int. Cl.**[6] **H01L 21/70**

[52] **U.S. Cl.** **438/787**; 438/787; 438/788; 438/773; 438/981; 438/257; 438/263; 438/264; 438/267; 438/211; 438/216; 438/119; 438/593; 148/DIG. 117; 148/DIG. 163

[58] **Field of Search** ..... 438/773, 981, 438/211, 216, 199, 257, 263, 264, 787, 788, 593, 594, 267; 148/DIG. 163, DIG. 117

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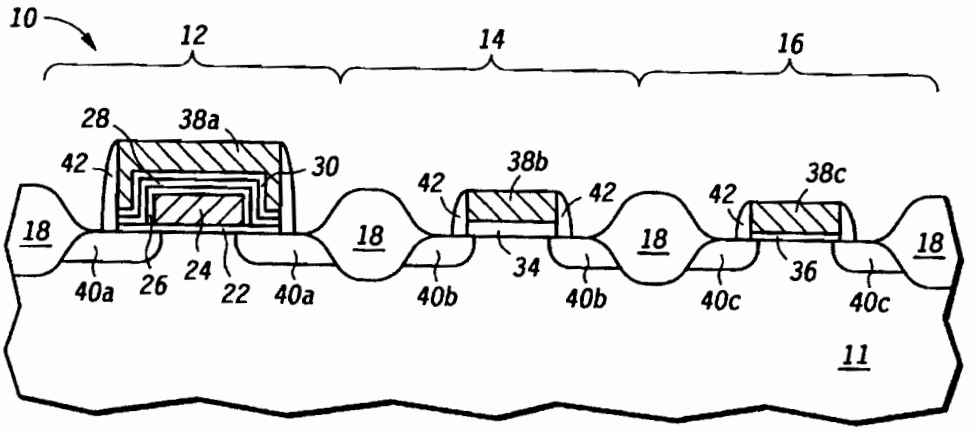
Primary Examiner—Charles Bowers
Assistant Examiner—Thanh Nguyen
Attorney, Agent, or Firm—J. Gustav Larson; Keith E. Witek

[57] **ABSTRACT**

A method for form an integrated circuit device begins by growing a tunnel oxide **(22)**. The tunnel oxide is exposed to a nitrogen containing ambient whereby nitrogen is incorporated at atomic locations at the interface between the tunnel oxide **(22)** and a substrate **(11)**. This tunnel oxide and nitrogen exposure is performed for all of a floating gate active area **(12)**, a high voltage active area **(14)** and a logic gate active area **(16)**. A floating gate electrode **(24)** and interpoly dielectric regions **(26** through **30)** are then formed in the floating gate region **(12)**. The tunnel oxide **(22)** is etched from the active areas **(14** and **16)** whereby nitrogen contamination **(32)** may remain. An optional sacrificial oxidation and a low temperature 830° C. wet oxidation process utilizing HCL, H2 and O2 is then used to grow a high voltage gate dielectric **(34)** which has been shown to improve charge to breakdown characteristics by a factor of 1,000. After the formation of the high voltage gate oxide **(34)**, a lower voltage logic gate oxide **(36)** is then formed.

32 Claims, 3 Drawing Sheets



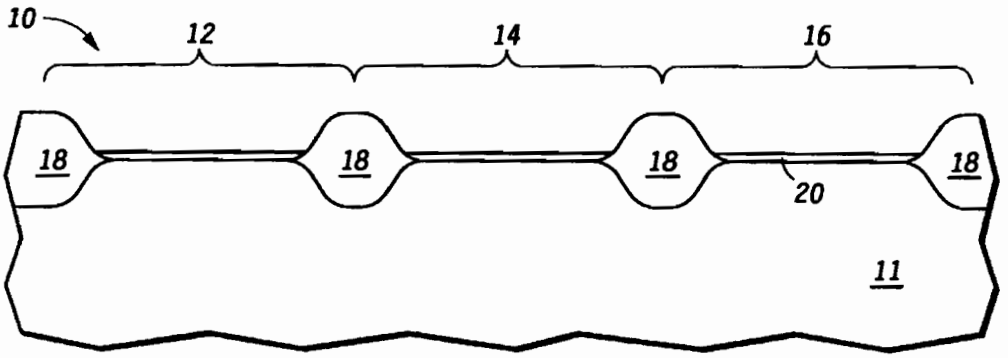


FIG.1

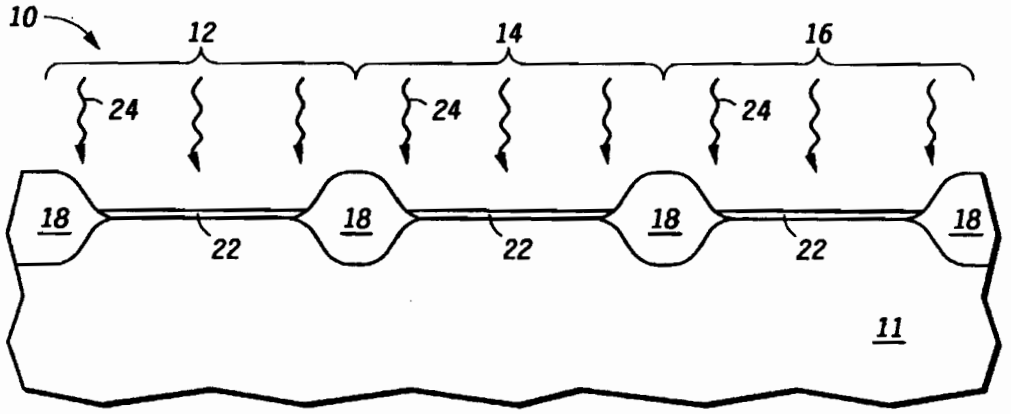


FIG.2

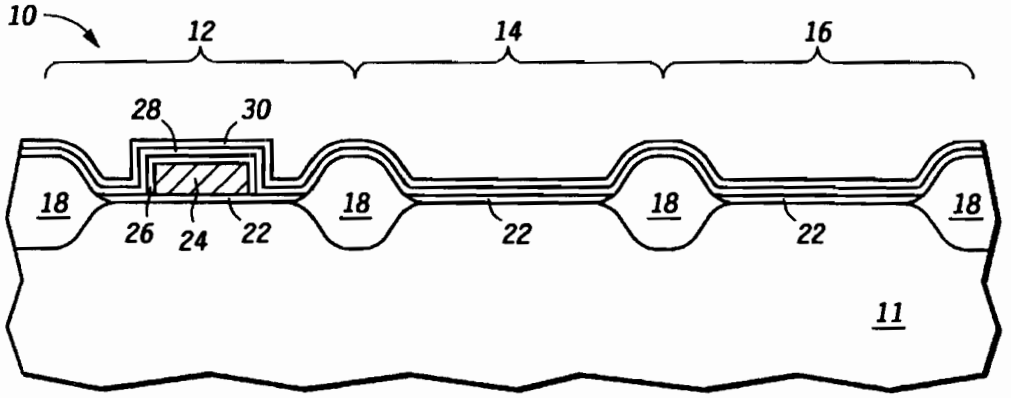


FIG.3

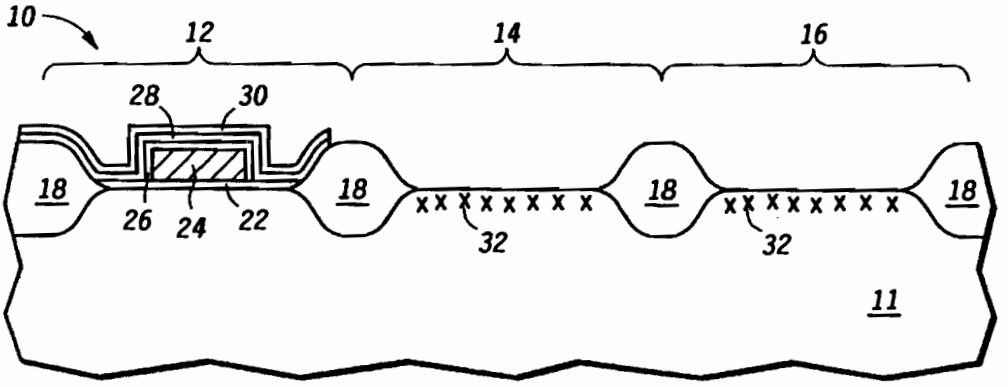


FIG.4

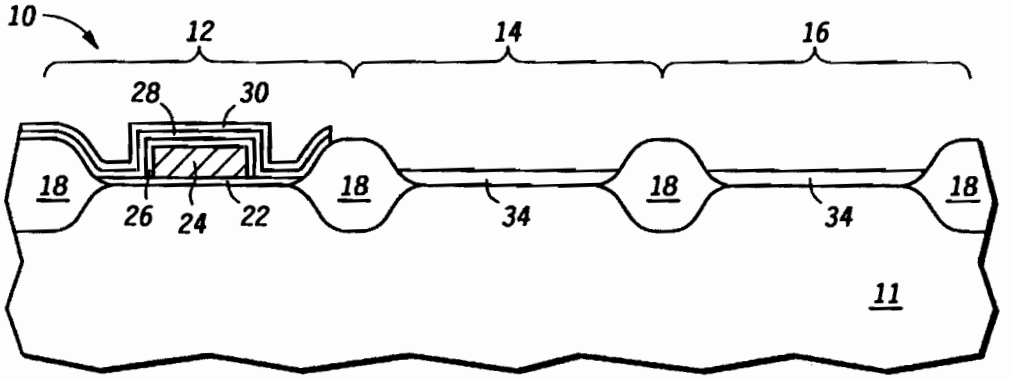


FIG.5

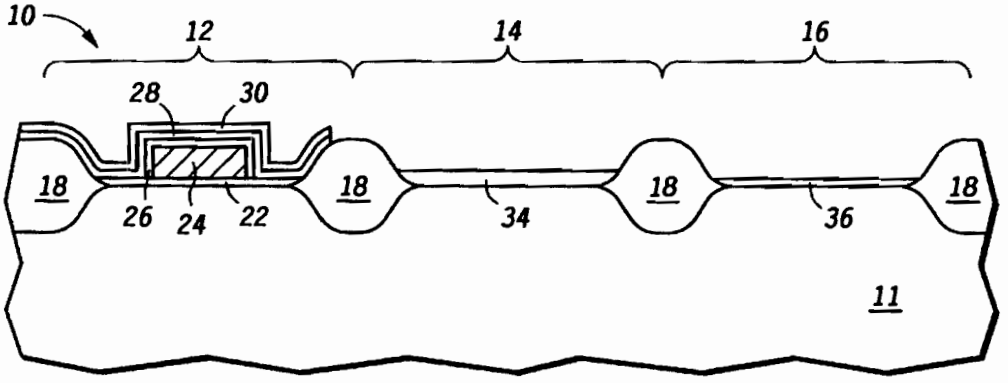
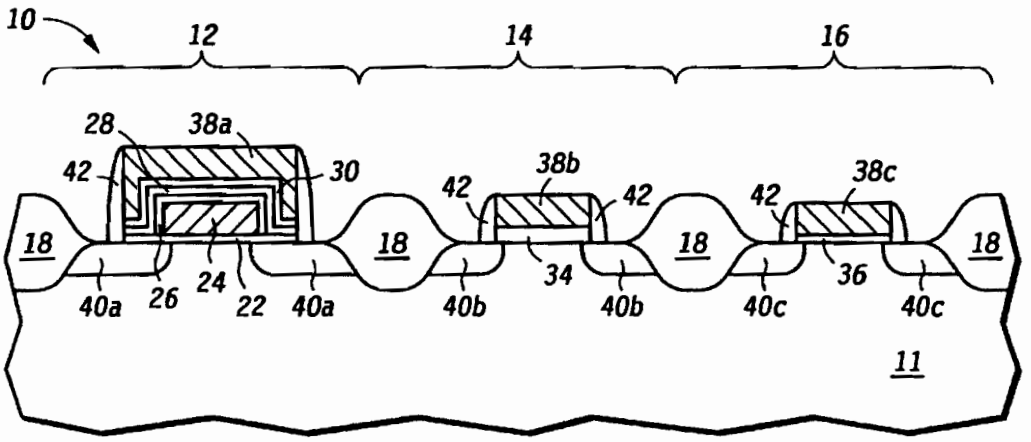


FIG.6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38c
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40a
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40c
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FIG. 7

METHOD FOR FORMING A HIGH VOLTAGE GATE DIELECTRIC FOR USE IN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The present invention relates generally to semiconductor manufacturing, and more particularly to, forming a high voltage gate oxide for use in integrated circuits (ICs)

BACKGROUND OF THE INVENTION

The integrated circuit (IC) industry is continually striving to manufacture more robust gate dielectric materials for electrical devices. In the industry, advances in tunnel oxide formation and performance have been particularly desired. The tunnel oxide is typically the most-stressed oxide during electrical operation, and is typically a thin oxide of 90 angstroms or less in thickness. Due to its high level of stressing during operation and its thinness, the tunnel oxide needs to be made robust in order to improve integrated circuit (IC) yield and reliability. In order to improve the robustness of the tunnel oxide in a floating gate memory cell, the integrated circuit industry has exposed tunnel oxide gate dielectrics to a nitrogen-containing ambient. The nitrogen in this ambient provides nitrogen atoms which penetrate the tunnel oxide and chemically bond at the oxide-to-substrate interface whereby the tunnel oxide performance is improved.

However, the industry is continually striving to integrate more types of devices onto a single silicon substrate whereby the gate oxide optimization for one device may adversely effect another gate oxide for different device. The nitrogen exposure process which is used to form conventional tunnel oxides for floating gate structures, while enhancing the performance of tunnel oxides, will greatly degrade the stability and performance of other oxides subsequently formed in logic gate regions and high voltage regions on the same substrate.

The reason nitrogen anneals used for floating structures results in degradation of subsequently formed high voltage and low voltage gate oxides is due to the fact that the nitrogen is also incorporated into the logic and high voltage areas of the substrate as well as the tunnel oxide portions of the substrate. These nitrogen atoms, which are resident at the interface of the substrate and oxide, result in subsequent etch processing being complicated and less uniform. In addition, oxide growth from these nitrogen containing surfaces to form high voltage oxides and low voltage logic gate oxides will result in a substantially non-planar oxide surface which has increased electric fields and therefore, reduced breakdown resistance. In addition, the nitrogen atoms from the substrate may be incorporated into the bulk of subsequently-grown thermal gate oxides whereby trap sites are formed in the bulk of these oxide layers. The bulk trap sites can adversely effect leakage current between the gate and the substrate, may affect threshold voltage, and will also affect the breakdown voltage of the high voltage and logic device.

One method which can be utilized to remove impurities from a substrate before thermal oxidation is the use of a sacrificial oxide layer. A dry sacrificial oxide layer is grown on the surface of the substrate and then etched using a wet etch. The combination of the sacrificial oxidation process and the wet etching reduces impurities at the surface of the substrate where subsequent thermal oxidation is to occur. However, sacrificial oxides add an additional growth step and etch step to the process. Sacrificial oxides may increase the thermal budget of the overall process, and may not be able to remove all of the nitrogen contamination from the substrate whereby the planarity of the thermally grown oxide is affected and breakdown voltage is reduced. In addition, too many sacrificial oxide processes in one process flow will thin field oxide isolation regions or trench fill material whereby device-to-device isolation across the integrated circuit (IC) is adversely affected. Therefore, the use of dry sacrificial oxides alone is not comprehensive enough to completely remove all of the nitrogen-doping problems associated with highly integrated products which utilize floating gates with nitrogen doped tunnel oxides.

A process known as wet oxidation has been used in the art for the formation of logic gate structures. Wet oxidation, however, is viewed as disadvantageous since wet oxidation provides a faster growth rate, which tends to be harder to control, than dry oxidation which has become the industry standard for gate oxidation. In addition, wet oxidation may increase the number of traps in the oxide layer. There is currently no known data showing that any wet oxidation would improve the breakdown voltage of high voltage oxides grown in areas which have previously been exposed to nitrogen atoms. There is further no known literature stating that high voltage products can be manufactured using wet oxidation whereby nitrogen-exposed tunnel oxides can also be integrated with these high voltage devices at a high performance level.

Therefore, there is a need in the IC industry for a new gate oxidation process which can be easily integrated to form ICs containing one or more of logic devices and/or high voltage devices along with floating gate arrays. In addition, this new gate oxide process should have a reduced thermal budget, improved or maintained transistor breakdown voltage operation, and improved charge-to-breakdown (Qbd), whereby gate oxide planarity is improved (reducing electric field strength across gate oxide) and nitrogen doping in the bulk of the oxide is also reduced. Furthermore, this new oxidation process should be capable of being utilized without sacrificial oxide processing, whereby field oxide isolation is not adversely eroded.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a cross sectional view of a substrate having three active areas separated by isolation regions;

FIG. **2** illustrates in cross sectional view an oxide being formed on the substrate of FIG. **1**;

FIG. **3** illustrates in cross sectional view the substrate of FIG. **2** having a floating gate and an ONO layer;

FIG. **4** illustrates in cross sectional view nitrogen contamination on the substrate following an etch process;

FIG. **5** illustrates in cross sectional view an oxide grown on the substrate;

FIG. **6** illustrates in cross sectional view the substrate following removal and reformation of a portion of the gate dielectric;

FIG. **7** illustrates in cross sectional view the substrate having a second gate structure.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the drawings have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the drawings to indicate corresponding or analogous elements.

DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention is a process for forming a nitrided tunnel oxide for a floating gate memory cell, a

thicker gate oxide for a high voltage logic device, and a thinner gate oxide for use in logic arrays, all on a single integrated circuit (IC) substrate. The process begins by forming a tunnel oxide over a floating gate portion of the substrate. The tunnel oxide is exposed to a nitrogen-containing ambient to incorporate nitrogen in the tunnel-oxide-to-substrate interface to improve tunnel oxide reliability. However, this tunnel oxide formation and nitrogen doping will also occur in the logic gate areas and the high voltage circuitry areas of the substrate. It has been found that this incorporation of oxynitride materials or nitrogen atoms into these logic and high voltage portions of the substrate is disadvantageous since subsequent gate oxide growth in these regions has topographical roughness and nitrogen incorporation in the bulk of the grown oxides, which forms trap sites. The trap sites along with the non-planar surface of the oxide-silicon interface will significantly reduce the charge to breakdown, Qbd.

In the process taught herein, the oxynitride tunnel oxide material (a nitride) is removed from the high voltage areas of the substrate and the logic gate areas of the substrate. An optional sacrificial gate oxide process may be used after oxynitride removal to perform a pre-clean of the substrate surface before gate oxidation. An 830° C. wet oxidation having an ambient comprised of O_2, and H_2 is then used to grow a thick gate oxide over both the logic gate regions and the high voltage regions. It has been shown that the use of this 830° C. wet oxidation process has the unexpected benefit of increasing the charge to breakdown value (Qbd) between the high voltage gate electrode and the substrate by a factor of roughly 1,000, wherein dry oxidations and high temperature wet oxidations do not have this benefit.

After formation of this thicker high voltage gate oxide, the logic gate portion of the substrate is etched free of this thicker gate oxide and a thinner logic gate dielectric layer is formed by any conventional process. The final result is that an IC device is formed wherein the non-volatile floating gate devices, the high voltage logic devices, and the thin gate oxide logic devices reside on the same substrate. In this integrated IC device, the formation of the nitrogen doped tunnel oxide has not adversely affected the high voltage gate oxide regions or logic gate oxide regions.

The process taught herein will have a reduced thermal budget compared to the dry oxidation processes taught by the prior art due to reduced oxidation temperatures. In addition, the wet oxidation process uses oxygen and hydrogen, preferably in molecular form, at a temperature of less than 880° Celsius. At this temperature, it has been shown to improve the planarity of the thermally grown high voltage gate oxide while simultaneously reducing the nitrogen that is incorporated into the bulk of the high voltage gate oxide. The wet process taught herein for high voltage gate oxides also reduces problems due to residual nitrogen-related materials in the logic gate areas even if the high voltage wet gate oxide is totally removed from this area before logic gate oxide growth. Both this reduction of nitrogen in the bulk and the improved planarity of this thermally grown high voltage oxide has been shown to greatly improve charge to breakdown (Qbd) of the high voltage device by a factor of roughly 1,000. In general, the gate oxide taught herein allows for high voltage (5 volt–18 volt) operation without adverse breakdown effects. The process taught herein is easily integratable with other processes such that floating gate devices, high voltage devices, and logic gates may be readily manufactured on a single integrated circuit substrate with or without nitrogen doping of some of these gate oxides.

The invention can be further understood with reference to FIGS. 1–7.

FIG. 1 illustrates an integrated circuit device **10**. Integrated circuit device **10** has a substrate **11**. Substrate **11** is preferably a silicon wafer. However, substrate **11** can be gallium arsenide, a germanium-based substrate, silicon on insulator (SOI) material, and the like. Field oxide isolation regions **18** are illustrated as being formed over the surface of the substrate **11** in FIG. **1**. Although FIG. **1** illustrates that the field isolation regions **18** are local oxidation of silicon (LOCOS) structures, other technologies such as shallow trench isolation (STI) or polysilicon encapsulated local oxidation of silicon (PELOX) could be used. In FIG. **1**, the formation of field oxide isolation regions **18** creates a plurality of active areas across the surface of substrate **11**. FIG. **1** specifically illustrates three such active areas **12**, **14** and **16**. A first active area **12** of FIG. **1** is an active area which will be used to form floating gate structures such as EEPROM memory cells, EPROM memory cells, and/or flash EEPROM memory structures. A second active area **14** in FIG. **1** is an active area which is used form high voltage transistors for I/O buffers and to form the logic which applies program and erase voltages to the floating gate arrays. A third active region **16** in FIG. **1** is a region which is used to form lower voltage transistors for high performance logic purposes, such as the formation of microcontroller core.

FIG. **1** also illustrates that a sacrificial oxide is formed overlying the three active areas **12**, **14** and **16**. The layer **20** is typically formed by dry oxidation at roughly 900° C. for roughly one hour. The sacrificial oxide **20** in FIG. **1** is grown to consume impurities at the top surface of the semiconductor substrate **11**. In addition, crystalline silicon defects at the surface of the substrate **11** may be reduced by the formation of the sacrificial oxide **20**. In addition, the layer **20** provides a screen oxide through which ion implantation can readily occur, and may also improve a planarity of the overall surface of the substrate. After formation of the sacrificial oxide layer **20**, a wet chemistry is used to remove the sacrificial oxide from the surface of the substrate **11**. It should be noted that a selective tunnel oxide area etch can be used as well.

FIG. **2** illustrates that a tunnel oxide layer **22** is formed after the removal of the sacrificial oxide **20** of FIG. **1**. The tunnel oxide **22** is a thermally grown oxide formed via a dry or wet O_2 growth ambient. The oxide **22** is typically grown to a thickness of 90 angstroms or less which is required in order to enable sufficient electron tunneling. Either after formation of the oxide **22** or in situ during formation of the oxide layer **22**, the oxide layer **22** is exposed to a nitrogen-containing ambient **24**. The nitrogen-containing ambient **24** will provide atomic nitrogen, and like species, to the tunnel-oxide-to-substrate interface either through thermal diffusion or through ion implantation. Typically, the tunnel oxide **22** is placed in a furnace and exposed to one or more of N_2, NO, NH_3, or N_2O, with N_2O being the preferred nitrogen carrier. The exposure of the oxide **22** to the nitrogen ambient **24** will result in nitrogen atoms being incorporated into the substrate-to-tunnel-oxide interface in all of the regions **12**, **14** and **16**.

In FIG. **3**, a first layer of polysilicon is deposited overlying the substrate **11**. This polysilicon layer may be insitu doped with phosphorus or like N-type dopant atoms or may be ion implanted with these impurities. This first layer of polysilicon is patterned and etched in a conventional manner in order to form a floating gate electrode **24** as illustrated in the active area **12** of FIG. **3**. After formation of the floating

gate structure **24**, a thermal oxidation process or a chemical vapor deposition (CVD) step is used to form an oxide layer **26**. The specific inter-polysilicon dielectric shown in FIG. **3** is an oxide-nitride-oxide (ONO) stack, however, dielectrics used in inter-polysilicon floating gate structures are typically comprised of thermal SiO_2, poly-oxide, silicon nitride, germanium oxide, germanium nitride, tetraethylorthosilicate (TEOS), and/or high temperature oxide of dichlorosilane and N_2O. A typical thickness of the oxide layer **26** is roughly 60–200 angstroms. After formation of the layer **26**, a chemical vapor deposition (CVD) process is utilized to deposit a silicon nitride layer **28**. A typical thickness of this silicon nitride layer **28** is roughly 60–150 angstroms. After formation of the nitride layer **28**, a thermal oxidation process or a chemical vapor deposition step is then utilized to deposit a silicon dioxide (SiO_2) layer **30** over a top of the silicon nitride layer **28**. A typical thickness of this layer **30** is roughly within the range of 20 angstroms to 100 angstroms. Collectively, the layers **26**, **28** and **30** form an inter-polysilicon ONO layer which will lie between the floating gate **24** and a subsequently formed control gate of the floating gate structure in region **12**.

Conventional lithographic patterning and etch processing are then used to remove the ONO layers **26–30** from the active areas **14** and **16** as illustrated in FIG. **4**. In addition, the nitrogen doped tunnel oxide **22** is also removed from the active areas **14** and **16** as illustrated in FIG. **4**. It is important to note that the layer **22** comprises a significant nitrogen concentration at the interface to the substrate **11**. The etch processing used to removed the oxide layer **22** is not optimized to fully remove the nitrogen-containing interface at the top surface of the substrate **11**. Conventional and known oxide etches do not adequately etch nitrogen doped regions by design. Therefore, even after the etching of these layers of material **22**, **26**, **28**, and **30**, some nitrogen contamination **32** may still remain in the active areas **14** and **16**. As previously discussed, any thermal oxidation process which is performed in regions **14** and **16** with the presence of these nitrogen contamination sites **32** will result in a non-planar gate oxide interface and nitrogen incorporation into the bulk of the thermal gate oxide. This non-planar surface and nitrogen bulk incorporation results in the charge to breakdown (Qbd) of the devices in regions **14** and **16** being adversely affected.

Therefore, an optional sacrificial gate oxide process similar to the sacrificial gate oxide process illustrated in FIG. **1** may be utilized again in FIG. **4** in an attempt to reduce some of the nitrogen contamination **32** at a surface of the substrate. In addition, the sacrificial gate oxide used at this step in the process may be grown using the process taught for the subsequent layer **34** as taught in FIG. **5**. In other words, both the sacrificial oxide and the gate oxide **34** of FIG. **5** may be formed using a low temperature 830° C. wet oxidation comprising an ambient of O_2, and H_2. Therefore, the robust nitrogen removing properties of the wet oxide taught herein (in more detail in subsequent figures) can be utilized for sacrificial oxide steps to further the benefits of this process. Therefore, as long as a single wet oxidation step of regions **14** and **16** is performed either in a sacrificial capacity or in a gate oxide capacity will reduce nitrogen effects on the final gate oxide quality. In addition, it is further advantageous to use a subsequent thermal growth process, in addition to the sacrificial oxidation or in lieu of the sacrificial oxidation, to further provide the nitrogen-removing properties taught herein.

FIG. **5** illustrates that a 220–350 angstrom thick wet oxide **34** is grown over the active areas **14** and **16**. It should be understood that the thickness of the layer **34** could be any thickness greater than approximately 100 angstroms depending upon the high voltage application. In order to form the layer **34**, the substrate is elevated to a temperature less than 880° C. and preferably to temperature of 830° C. While at this temperature, the substrate is exposed to O_2 and H_2. In a preferred form, the concentration of hydrogen to oxygen in this ambient is 60% to 40%. However, the ratio of hydrogen atoms to oxygen molecules can be anywhere within the range of 7:3 to 2:8 and will still result in at least some of the benefits taught herein.

It has been shown that the use of the 830° C. wet oxidation process, previously described as forming the layer **34**, will result in a substantially planar thermal oxidation which is improved over the prior art. This more planar surface results in lower electric field strength and improves the charge to breakdown (Qbd) characteristics of transistors. Furthermore, nitrogen incorporation from the contamination **32** into the bulk of layer **34** has also been reduced. This reduction in nitrogen contamination reduces trap sites in the bulk of the oxide **34** whereby high voltage transistor performance is enhanced. In addition, the process taught herein uses a low temperature 830° C. wet process which improves a thermal budget over prior art higher-temperature dry gate oxidation processing. In addition to improved charge to breakdown operation and improved thermal budget, the transistors formed within the active area **14** can operate easily within the range of 5 volts to 18 volts without adverse effects. As can be seen via FIGS. **1–5**, the process taught herein is easily integrated into microcontroller processes which contain floating gate structures, high voltage structures, and/or logic gate devices on an highly-integrated IC.

Furthermore, the oxide **34** has been shown to have the unexpected benefit of improving charge to breakdown (Qbd) characteristics of the high voltage devices by a factor of 1,000. It has further been shown that thermal oxidation of the layer **34** at a temperature of roughly 900° C. will not obtain this factor of 1,000 improvement in the charge to breakdown properties. Therefore, it is advantageous to perform this thermal oxidation below roughly 880° C. and specifically at below roughly 880° C. in order to achieve optimal thicknesses (250 angstroms –350 angstroms) while simultaneously achieving the extensive 1000× reduction in the adverse affects of the nitrogen presence. Conventional integrated circuit (IC) wisdom suggests that as oxidation temperature increases, the more improved the characteristics of the oxide will become. Therefore, the factor of 1,000 improve in the charge to break down characteristics of the gate oxide **34** is an unexpected benefit, and is contrary to conventional teachings in the integrated circuit (IC) art.

FIG. **6** illustrates that conventional masking and etching processes are used to remove the thicker oxide **34** from the substrate portion **16**. It is important to note that the contamination **32** illustrated previously in FIG. **4** will not now adversely effect the dry oxidation of the region **16** due to the previous oxidation of region **16** via layer **34** in FIG. **5**. Due to the previous oxide **34** being formed over the region **16** in FIG. **5**, the Qbd effects of the sites **32** of FIG. **4** have been reduced not only in the region **14**, but also in the region **16** of FIG. **6** even after removal of the layer **34** in FIG. **6**. Therefore, conventional dry oxidation processing can be utilized to form a thin (120 angstroms or less) gate dielectric region **36** in the logic gate portion **16** of FIG. **6** whereby oxide planarity and bulk incorporation of nitrogen into the gate oxide **36** is also improved as was the case for the oxide layer **34** of region **14**.

FIG. **7** illustrates that a second polysilicon layer is deposited overlying the substrate **11**. Conventional lithographic

and etching processing is used to define a control gate **38***a* which overlies the floating gate **24**, a high voltage control gate **38***b* which overlies a channel region within region **14**, and a logic control gate **38***c* which lies within the logic gate region **16** of FIG. **7**. After formation of the gates **38***a*–**38***c*, a TEOS deposition is performed and a reactive ion etch is performed in order to form oxide sidewall spacers **42**. In other forms, the sidewall spacers used to form source and drain regions can be silicon nitride or another type of dielectric or composite dielectric. In addition, lightly doped drain (LDD) regions can be formed herein. After formation of the spacers **42**, an ion implantation or thermal diffusion step is used to form source and drain electrodes **40***a*–**40***c* as illustrated in FIG. **7**. After formation of the source and drain electrodes **40***a*–**40***c*, conventional processing continues with the deposition or formation of both dielectric and conductive layers (e.g., overlying metal layers which couple to the transistors of FIG. **7**) until final passivation is eventually formed. The integrated circuit (IC) device is then diced from the wafer and packaged in a final integrated circuit structure for end-use.

It is important to note that FIG. **7** specifically illustrates a non-self-aligned floating gate process. It is possible to form the floating gate devices in the active area **12** using a self-aligned floating gate and control gate process. Also, the ion implants used to form the source and drain regions may be used to dope the second layer of polysilicon **38***a*–**38***c* to actively change the conductivity of these gate regions. Also, different ion implantation steps may be performed at different times that specifically illustrated herein. In other words, the implants into the region **12** may be totally different that the implants into one or more of the regions **14** and **16** via the use of ion implantation masking.

Although the invention has been described and illustrated with reference to specific embodiments, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that modifications and variations may be made without departing from the spirit and scope of the invention. For example, the process taught herein may be used for either complementary metal oxide semiconductor (CMOS) processing or bi-CMOS processing. The process taught herein can be used to integrate logic devices with floating gate device, high voltage devices with floating gate devices, or integrate all three of logic devices, high voltage devices, and floating gate devices on a single IC. The term "oxynitride" or "nitride" is used herein. These terms are intended to mean any oxide or nitride which is contaminated with nitrogen whether at the substrate-to-oxide interface or within the oxide itself. It should be noted that various inert carrier gases such as Argon may be used for process flows as described herein. The process used herein may also be used to reduce undesirable effects associated with fluorinated oxides as opposed to nitrided oxides. The O2 and H2 wet growth environments taught herein may also include HCl. Therefore, it is intended that this invention encompass all of the variations and modifications as fall within the scope of the appended claims.

What is claimed is:

1. A method for forming a semiconductor device, the method comprising the steps of:

providing a semiconductor substrate having a substrate surface;

forming an oxide on the semiconductor substrate;

exposing the oxide to nitrogen in order to form a nitride;

forming a floating gate electrode over the nitride;

removing the nitride from a first region of the semiconductor substrate;

forming a wet grown oxide over first region substrate, wherein the wet grown oxide is formed in an ambient including hydrogen and oxygen; and

forming a conductive gate over the wet grown oxide.

2. The method of claim **1**, wherein the step of forming a wet grown oxide further comprises forming the wet grown oxide at a temperature of less than 880° Celsius.

3. The method of claim **1**, wherein the step of forming a wet grown oxide further comprises forming the wet grown oxide at a temperature of less than approximately 840° Celsius.

4. The method of claim **1**, wherein the step of forming a wet grown oxide further comprises forming the wet grown oxide at a temperature of approximately 830° Celsius.

5. The method of claim **1**, wherein the step of forming a wet grown oxide further comprises the ambient including hydrogen molecules and oxygen molecules.

6. The method of claim **5**, wherein the step of forming a wet grown oxide introduces a ratio of hydrogen molecules to oxygen molecules (H2:O2) in a range of 7:3 to 2:8.

7. The method of claim **5**, wherein the step of forming a wet grown oxide introduces a ratio of hydrogen molecules to oxygen molecules (H2:O2) of approximately 6:4.

8. The method of claim **1**, wherein the step of forming a wet grown oxide further comprises the ambient including hydrogen chloride.

9. The method of claim **1**, wherein the step of forming a wet grown oxide further comprises the ambient including H2O steam.

10. The method of claim **1**, further comprising the steps of:

forming an oxide layer on the substrate surface prior to forming the wet grown oxide; and

removing the oxide layer prior to forming the wet grown oxide.

11. The method of claim **10**, wherein the step of forming the oxide layer comprises:

forming the oxide layer in a wet environment containing oxygen molecules, hydrogen molecules, and HCl at approximately 830° Celsius.

12. The method of claim **1**, further comprising the steps of:

forming a tunnel oxide region over a second region of the semiconductor substrate during the step of forming the nitride; and

forming a floating gate over the second region prior to the step of removing the nitride.

13. The method of claim **1**, further comprising the steps of:

removing the wet grown oxide from a second region of the semiconductor substrate prior to the step of forming a conductive gate;

forming a new oxide over the second region of the semiconductor substrate; and

wherein the step of forming a conductive gate includes forming a conductive gate over the second region of the semiconductor substrate.

14. The method of claim 13, wherein the step of forming a new oxide includes the new oxide having a different thickness than the wet grown oxide.

15. The method of claim **1**, wherein a thickness of the wet grown oxide is chosen to allow a transistor to operate with a gate voltage in a range of approximately 5 to 18 volts.

16. The method of claim 1, wherein a thickness of the wet grown oxide is approximately 100–350 wet oxide thickness.

17. A method for forming a semiconductor device, the method comprising the steps of:

providing a semiconductor substrate;

forming field isolation over the semiconductor substrate to form a first active region and a second active region;

forming an oxynitride in direct contact with the semiconductor substrate and over the first active region and the second active region;

forming a first conductive gate over the oxynitride in the first active region;

forming a dielectric layer over the first conductive gate;

removing the dielectric layer and oxynitride from the second active region following the step of forming the first conductive gate;

forming a wet grown oxide over the second active region, wherein the wet grown oxide is formed in an ambient including hydrogen and oxygen; and

forming a second conductive gate over the first conductive gate and a third conductive gate in the second active region.

18. The method of claim 17 wherein the step of forming a second conductive gate over the first conductive gate comprises:

forming a device wherein the second conductive gate is a gate electrode for a non-volatile storage device, and the device including the third conductive gate is gate electrode for a high voltage logic device.

19. The method of claim 17 wherein the step of forming a second conductive gate over the first conductive gate comprises forming a device wherein the second conductive gate is used to form a non-volatile storage device the third conductive gate is used to form a logic device.

20. The method of claim 17, wherein the step of forming a wet grown oxide further comprises forming the wet grown oxide at a temperature of approximately 830° Celsius.

21. The method of claim 17, wherein the step of forming a wet grown oxide introduces a ratio of hydrogen molecules to oxygen molecules (H_2:O_2) of approximately 6:4.

22. The method of claim 17, wherein the step of forming a wet grown oxide further comprises the ambient including H_2O steam.

23. The method of claim 17, further comprising the steps of:

forming a sacrificial oxide layer using a wet process prior to forming the wet grown oxide; and

removing the sacrificial oxide layer prior to forming the wet grown oxide.

24. The method of claim 17, wherein a thickness of the wet grown oxide is chosen to allow a transistor to operate with a gate voltage in a range of approximately 5 to 18 volts.

25. A method for forming a semiconductor device, the method comprising the steps of:

providing a semiconductor substrate;

forming field isolation over the semiconductor substrate to form a first active region, a second active region, and a third active region;

forming an oxynitride over the first active region, the second active region, and the third active region;

forming a first conductive gate over the first active region and the oxynitride, the first conductive gate for functioning as a floating gate for a non-volatile cell;

forming a dielectric layer over the first conductive gate;

removing the oxynitride from the second active region and the third active region;

forming a wet grown oxide over the second active region and the third active region, wherein the wet grown oxide is formed in a wet oxidation ambient including hydrogen and oxygen;

removing the wet grown oxide over the third active region;

forming an oxide over the third active region; and

forming a second conductive gate over the first conductive gate which functions as a control gate for the non-volatile cell, a third conductive gate in the second active region to form a gate for another logic devices, and a fourth conductive gate in the third active region.

26. The method of claim 25, wherein the step of forming a second, third and fourth conductive gate further comprises:

forming a non-volatile device using the second conductive gate;

forming a first logic device using the third conductive gate; and

forming a second logic device using the fourth conductive gate, wherein the second logic device is for operating at a power supply voltage different than the first logic device.

27. The method of claim 26, wherein the first logic device is operates with a gate voltage in a range of approximately 5 to 18 volts.

28. The method of claim 26, wherein the second logic device is operates with a gate voltage in a range of approximately 0.9 to 5.0 volts.

29. The method of claim 25, wherein the step of forming a wet grown oxide further comprises forming the wet grown oxide at a temperature of approximately 830° Celsius.

30. The method of claim 25, wherein the step of forming a wet grown oxide introduces a ratio of hydrogen molecules to oxygen molecules (H2:O2) in a range of approximately 6:4.

31. The method of claim 25, wherein the step of forming a wet grown oxide further comprises the wet oxidation ambient including H2O steam.

32. The method of claim 25, further comprising the steps of:

forming a oxide layer using a wet process prior to forming the wet grown oxide; and

removing the oxide layer prior to forming the wet grown oxide.

* * * * *

Exhibit O

US005946177A

United States Patent [19]

Miller et al.

[11] **Patent Number: 5,946,177**

[45] **Date of Patent: Aug. 31, 1999**

[54] **CIRCUIT FOR ELECTROSTATIC DISCHARGE PROTECTION**

[75] Inventors: **James Wesley Miller; Cynthia Ann Torres; Troy L. Cooper**, all of Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **09/134,943**

[22] Filed: **Aug. 17, 1998**

[51] **Int. Cl.**[6] **H02H 9/00**

[52] **U.S. Cl.** **361/56**

[58] **Field of Search** 361/56, 91, 111

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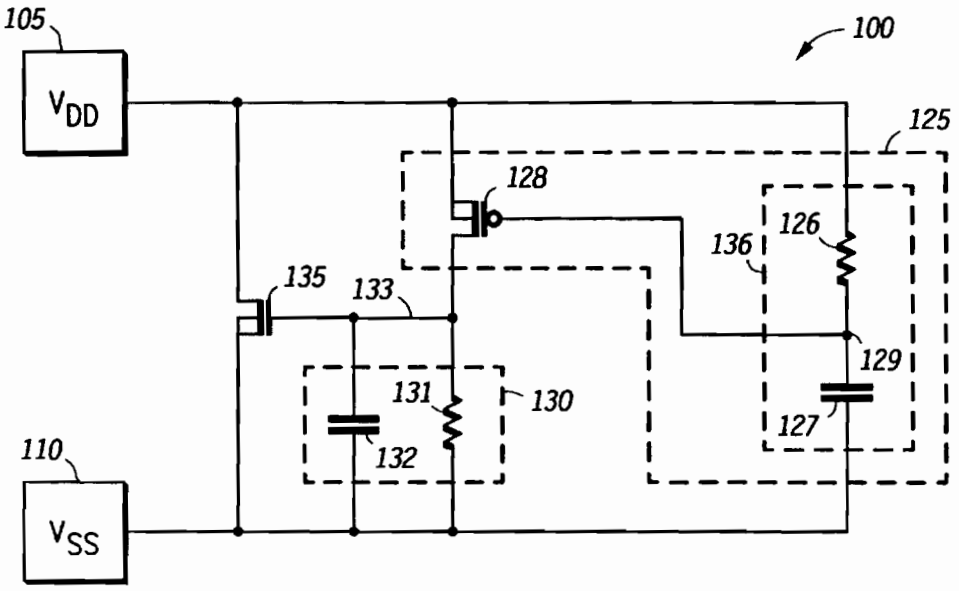
Primary Examiner—Ronald W. Leja
Attorney, Agent, or Firm—Robert L. King

[57] **ABSTRACT**

A circuit **(100)** ensures electrostatic discharge (ESD) protection during an ESD event. The ESD circuit **(100)** has a current shunting device **(135)**, a RC trigger circuit **(125)** and a RC delay circuit **(130)**. The shunting device **(135)** is connected between two IC power supply rails, and provides the primary current path for a positive ESD event referenced from one power supply rail (V_{DD} **105)** to the other (V_{ss} **110)**. The trigger circuit **(125)** initially activates the shunting device into a low resistance conductive state in response to an ESD event. The RC delay circuit **(130)** serves to maintain the shunting device in the conductive state, initially produced by the trigger circuit **(125)**, for the remaining duration of the ESD event. A large capacitor required to achieve the delay time in this RC circuit may be eliminated by utilizing the gate-to-body capacitance in the existing shunting device **(135)**.

18 Claims, 6 Drawing Sheets



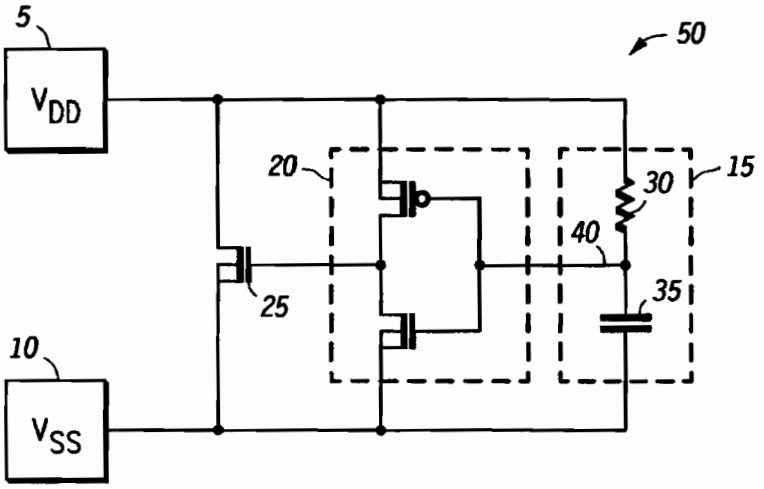


FIG.1
-PRIOR ART-

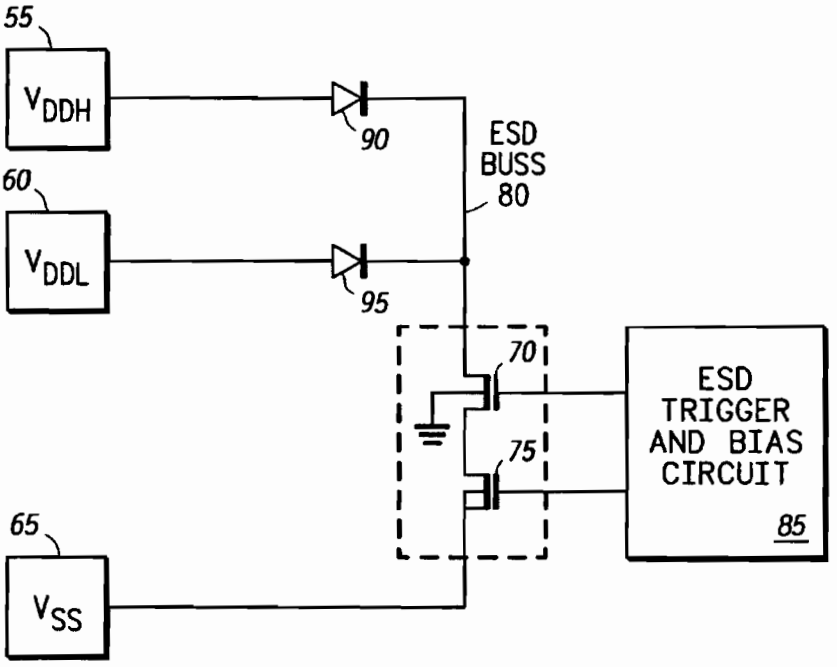


FIG.2
-PRIOR ART-

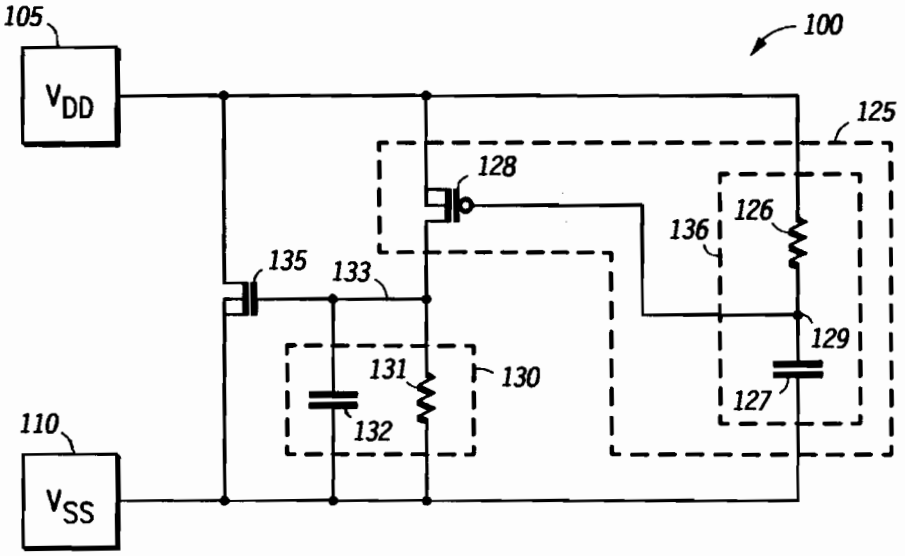

105
100
V_{DD}
125
128
126
136
135
133
129
131
130
127
132
110
V_{SS}

FIG. 3

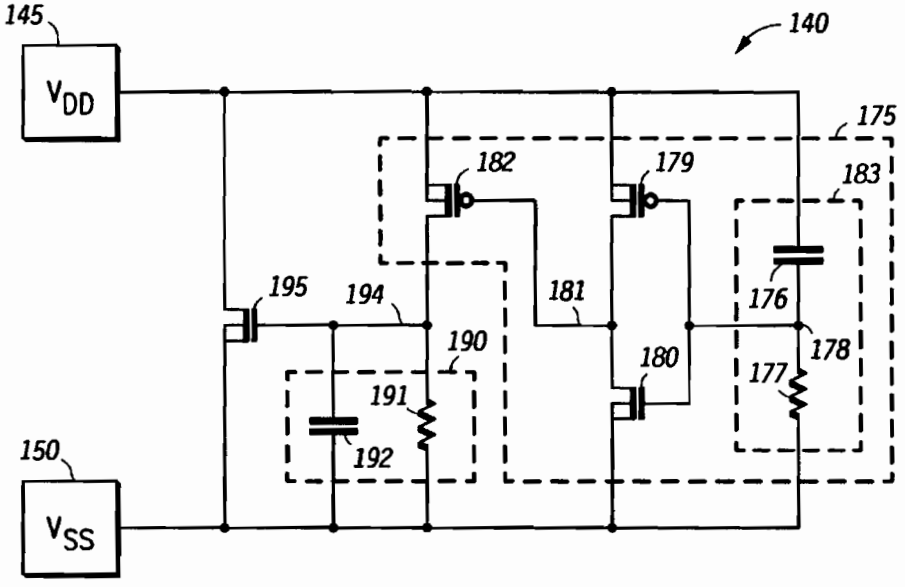

145
140
V_{DD}
175
182
179
183
195
194
181
176
190
180
178
191
177
192
150
V_{SS}

FIG. 4

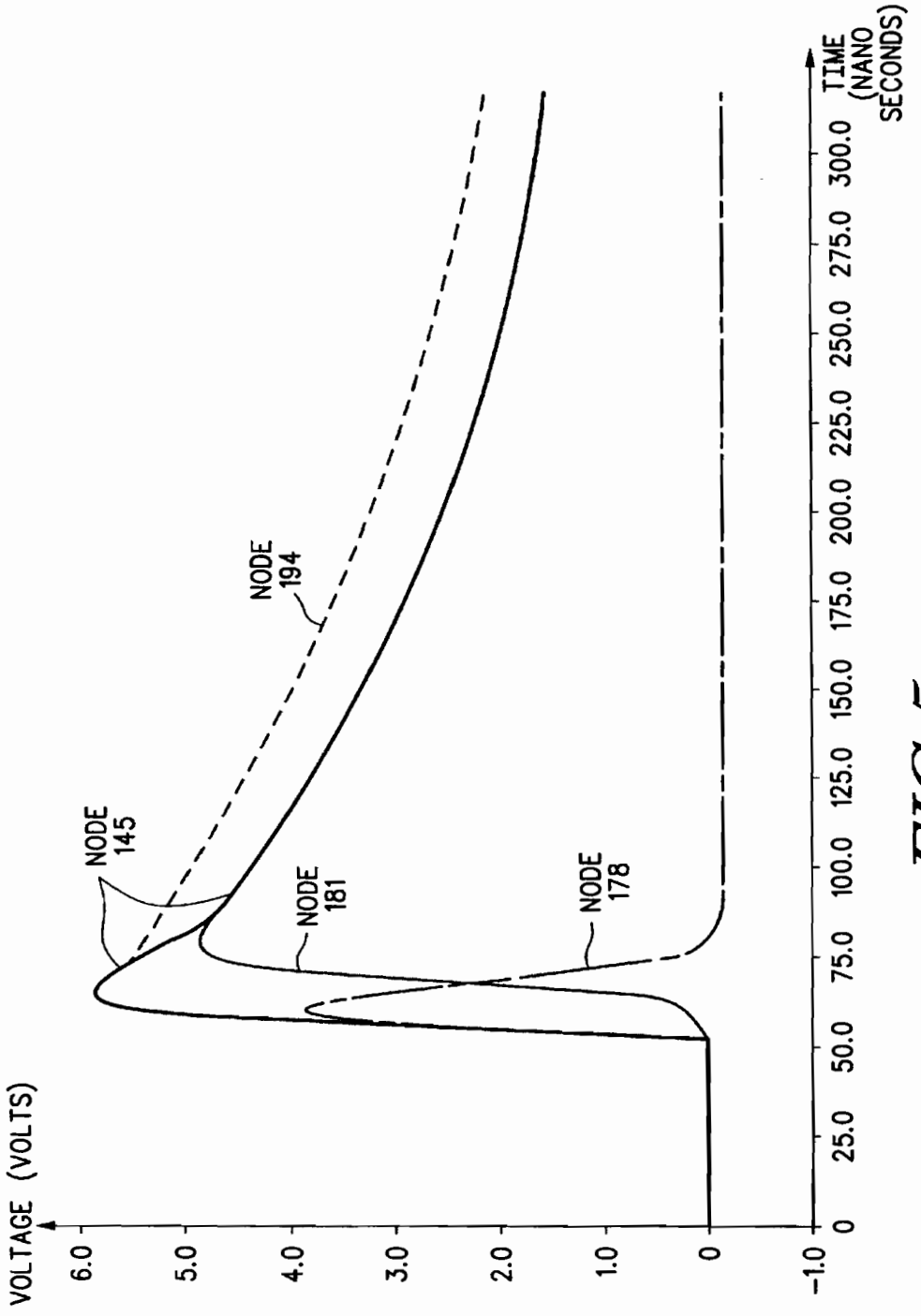

VOLTAGE (VOLTS)
6.0
5.0
4.0
3.0
2.0
1.0
0
-1.0
0
25.0
50.0
75.0
100.0
125.0
150.0
175.0
200.0
225.0
250.0
275.0
300.0
TIME (NANO SECONDS)
NODE 194
NODE 145
NODE 181
NODE 178

FIG. 5

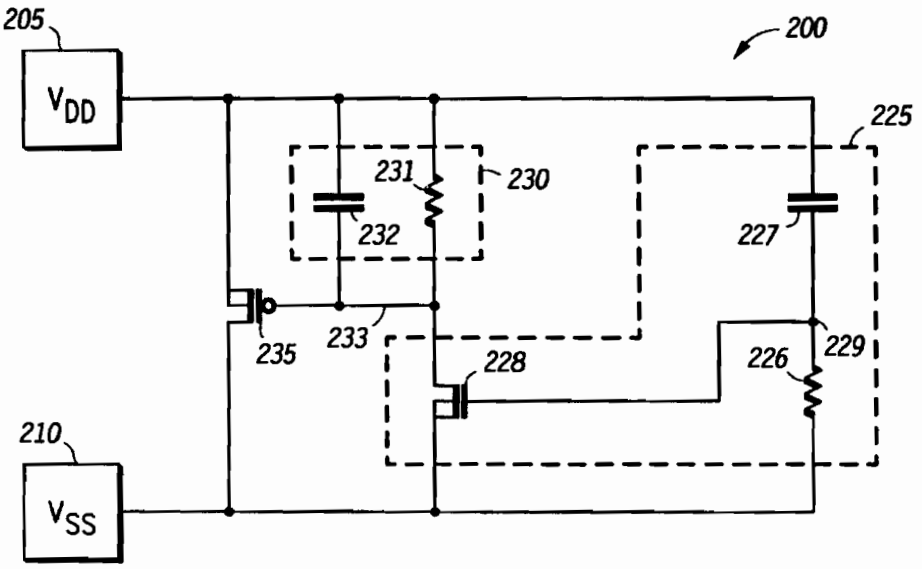

205
200
V_{DD}
225
231
230
232
227
235
233
228
226
229
210
V_{SS}

FIG. 6

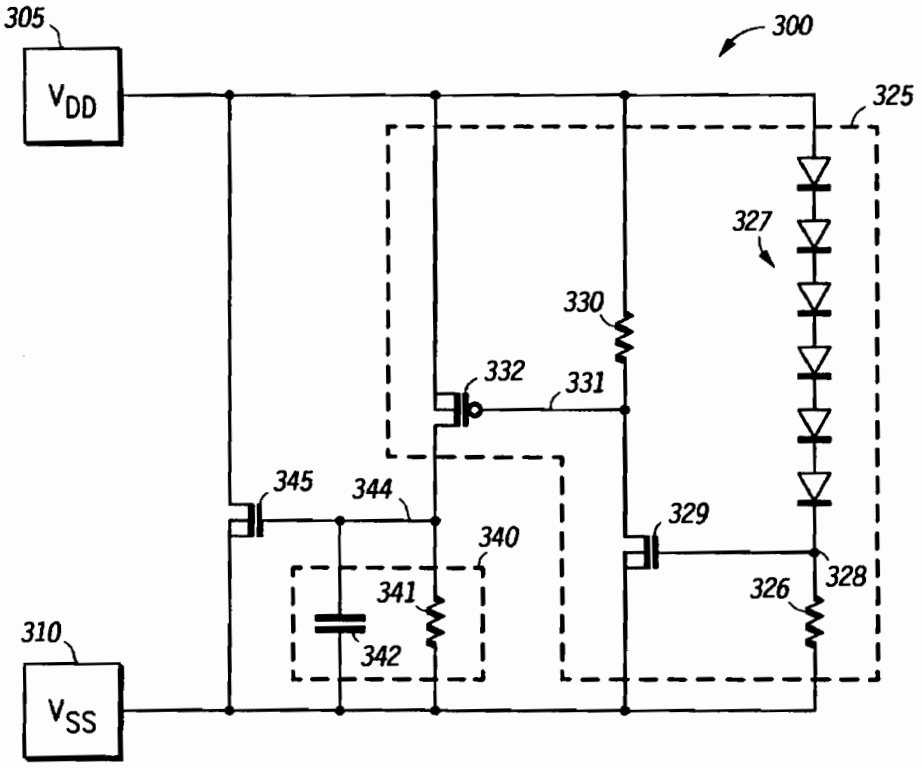

305
300
V_{DD}
325
327
330
332
331
345
344
329
340
328
341
326
310
342
V_{SS}

FIG. 7

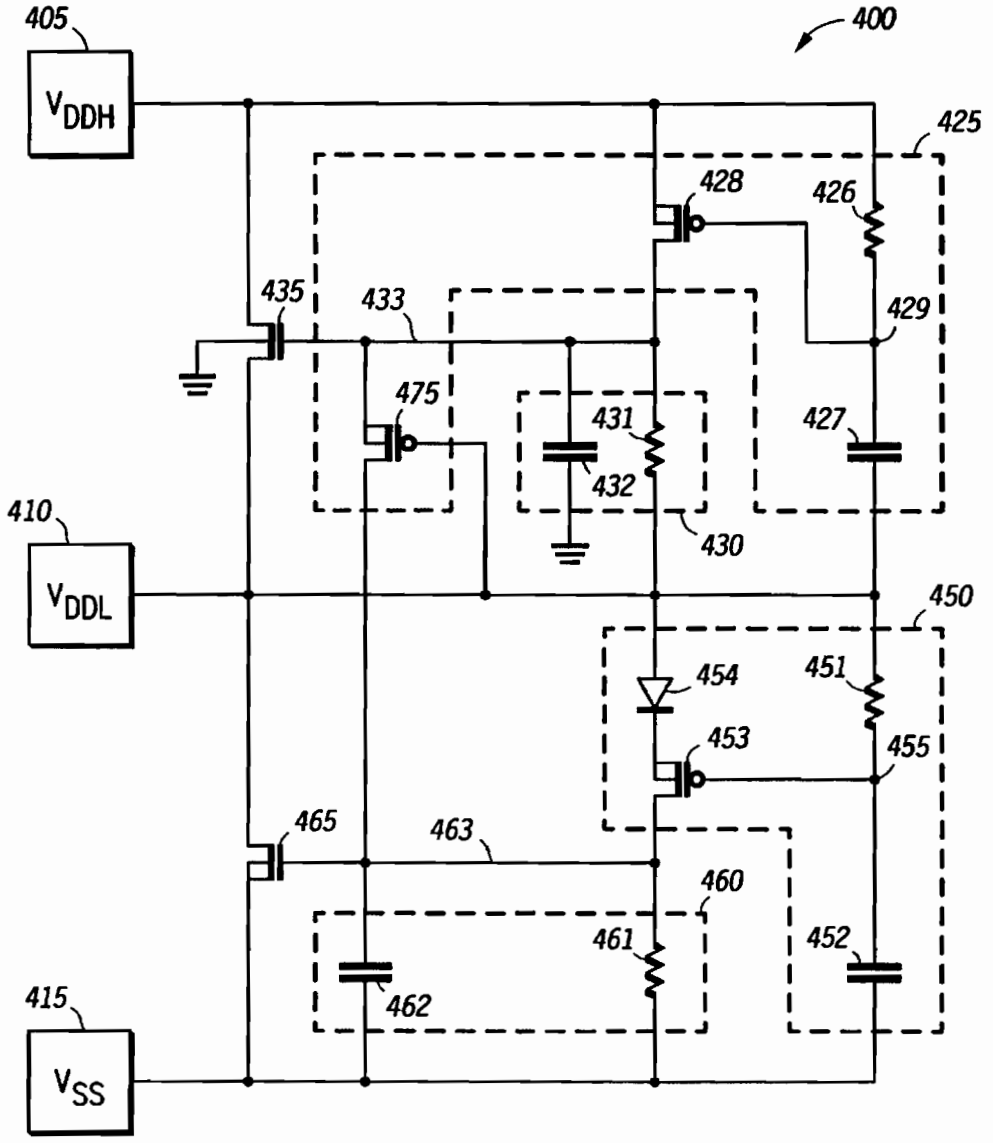

405
400
V_{DDH}
425
428
426
435
433
429
475
431
427
410
V_{DDL}
432
430
450
454
451
453
455
465
463
460
461
452
415
V_{SS}
462

FIG.8

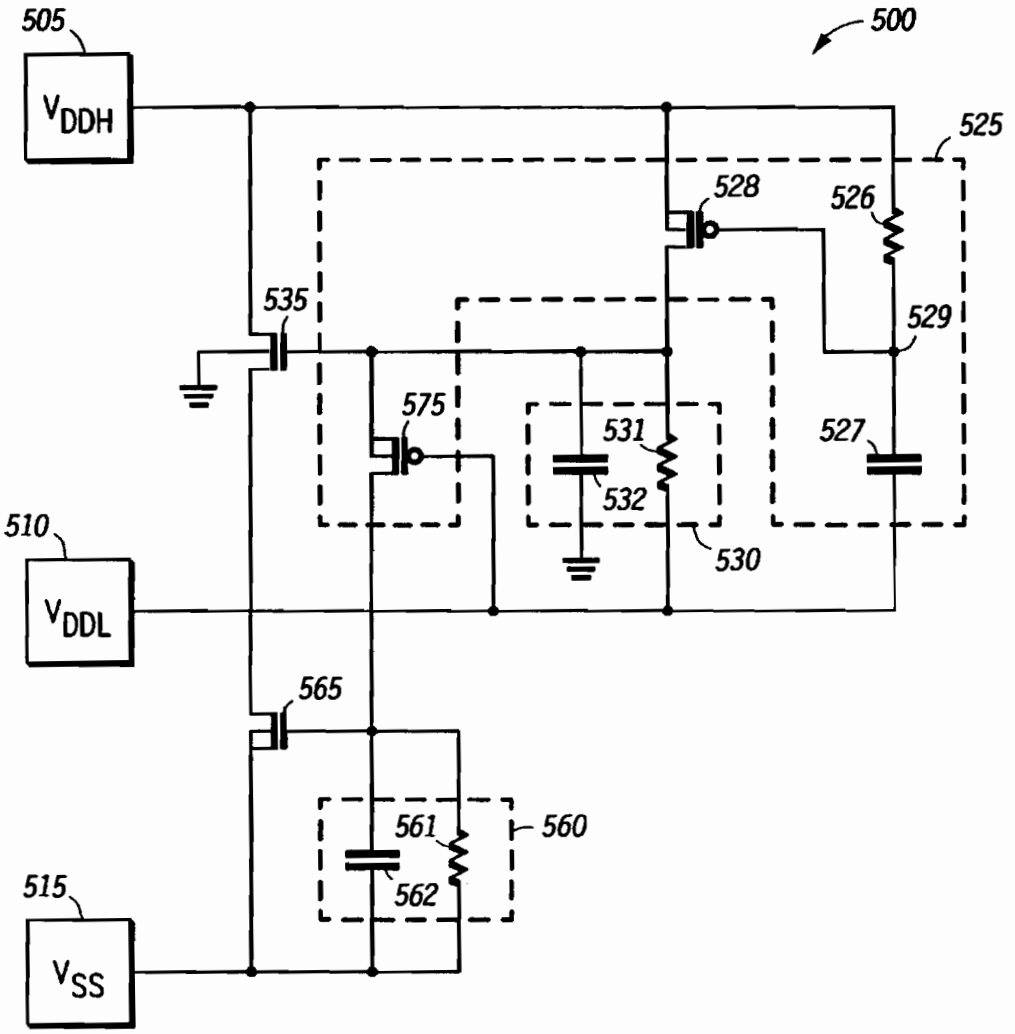

505
500
V_{DDH}
525
528
526
535
529
575
531
527
532
510
530
V_{DDL}
565
561
560
562
515
V_{SS}

FIG.9

CIRCUIT FOR ELECTROSTATIC DISCHARGE PROTECTION

FIELD OF THE INVENTION

The present invention generally relates to semiconductor circuits providing protection against electrostatic discharge (ESD) and electric overstress (EOS) events.

BACKGROUND OF THE INVENTION

In conventional integrated circuit (IC) ESD protection schemes, special clamp circuits are often used to shunt ESD current between the IC power supply rails and thereby protect sensitive internal elements from damage. A type of ESD clamp circuit, known as an active metal oxide semiconductor field effect transistor (MOSFET) clamp circuit, typically consists of three functional elements; a trigger circuit, a buffer stage, and a large MOSFET transistor. The trigger circuit is designed to respond to an applied ESD event but remains inactive during normal operation of the IC. The buffer stage is used to invert and amplify the trigger output in order to drive the gate terminal of the large MOSFET transistor. The large MOSFET transistor, connected between the two power supply rails, acts as the primary ESD current dissipation device in the clamp circuit. Active MOSFET clamp circuits typically rely on only MOSFET action to absorb ESD events, and since the peak current in an ESD event is on the order of amperes, large MOSFET transistor sizes are required.

A known RC-triggered active MOSFET ESD clamp circuit **50** is shown in FIG. **1**. The clamp circuit **50** in FIG. **1** protects a V_{DD} power supply rail **5** from positive ESD events referenced to a grounded V_{SS} power supply rail **10**. As shown in FIG. **1**, clamp circuit **50** employs a trigger circuit **15**, a buffer stage **20**, and a large N-channel MOSFET (NMOSFET) transistor **25**. Trigger circuit **15** is designed as a resistor-capacitor (RC) transient detector, utilizing resistor **30** and capacitor **35**. In response to an ESD event that induces a rapid positive voltage transient on the V_{DD} rail **5**, trigger circuit **15** initially holds a node **40** well below V_{DD}. The inverter stage **20**, with an input connected to node **40**, then drives the gate of NMOSFET **25** to V_{DD}. Once turned on, NMOSFET transistor **25** provides a low resistance shunt between the V_{DD} rail **5** and the VSS rail **10**. NMOSFET **25** will remain conductive for a period of time which is determined by the RC time constant of trigger circuit **15**. As a result, it is critical that this RC time constant is long enough to exceed the maximum expected duration of an ESD event, typically a few hundred nanoseconds, while short enough to avoid false triggering of the clamp circuit during normal ramp-up of the V_{DD} power rail, typically a few milliseconds. During normal operation of the IC, with a constant V_{DD} power supply level, NMOSFET **25** is biased in a nonconductive state.

A limitation with the clamp circuit of prior art FIG. **1** is that such a clamp circuit encompasses a large substrate area. The large size of NMOSFET **25** is unavoidable since the performance of an active MOSFET ESD clamp circuit is directly proportional to the channel width (dimension perpendicular to current flow) of this primary current dissipation device. The NMOSFET **25** channel length (dimension parallel to current flow) is typically set to the semiconductor process design rule minimum so as to achieve the minimum on-state resistance in the device. However, other portions of the clamp circuit, particularly the trigger circuit **15**, occupy a significant portion of the overall clamp area. The area utilized by trigger circuit **15**, including resistor **30** and capacitor **35**, commonly represents twenty to fifty percent of the area required for NMOSFET transistor **25**. Trigger circuit **15** requires this significant area in order to achieve the required RC time constant of a few hundred nanoseconds. Capacitor **35** is typically formed from a NMOSFET transistor with its source, drain, and body connected to V_{SS}, and its gate connected to node **40**. Resistor **30** is typically formed from a PMOSFET transistor with its source and body connected to V_{DD}, its drain connected to node **40**, and its gate connected to V_{SS}. PMOSFET resistor **30** is typically sized with a minimum channel width and maximum channel length so as to achieve the maximum possible device resistance. The limits for these dimensions are set by semiconductor process design rules in order to insure manufacturability and consistency in electrical characteristics. Therefore, in a given semiconductor process, there is a limit to the maximum resistance which may be achieved with PMOSFET resistor **30**. NMOSFET capacitor **35** must then be sized to produce the required RC time constant, with the typical result that this capacitor dominates the area utilized by trigger circuit **15**. A reduction in the size of trigger circuit **15**, particularly a reduction in the size of the NMOSFET capacitor **35**, would provide a more space efficient ESD clamp circuit.

Another limitation with the RC triggered clamp circuit of prior art FIG. **1** is susceptibility to false triggering during normal ramp-up of the V_{DD} power supply. These clamp circuits are at risk in IC applications where the V_{DD} power supply ramp-up time is on the order of the trigger circuit **15** RC time constant. ICs in battery powered applications may see a rapid rise in V_{DD} as the battery is connected. In addition, certain applications require ICs be inserted into powered up systems. This "hot-plugging" often results in a very rapid ramp-up of the IC V_{DD} power supply rail. Accordingly, there is a need for a clamp circuit which is more tolerant of a rapid ramp-up of the V_{DD} power supply.

In addition to the need to reduce the size and improve the performance of ESD clamp circuits, there is a further need to form more efficient rail clamp circuits that are capable of providing ESD protection for ICs having multiple power supply potentials. Many IC designs allow voltages in excess of the internal power supply voltage specified for a baseline process technology to be brought on board the chip. Protecting this higher voltage power rail can be achieved with stacked, or series-connected active MOSFET ESD clamp circuits. One such prior art circuit which utilizes stacked active MOSFET rail clamps is described in U.S. Pat. No. 5,654,862, assigned to Rockwell International Corporation and summarized in prior art FIG. **2**. This prior art circuit, shown schematically in FIG. **2** utilizes a stacked active MOSFET clamp circuit to protect multiple power rails. In FIG. **2**, three power supply rails are shown and labeled V_{DDH} **55**, V_{DDL} **60**, and V_{SS} **65**. A first NMOSFET **70** and a second NMOSFET **75** are serially connected between an ESD Bus **80** and the V_{SS} power supply rail **65**. The gate electrode of both NMOSFET **70** and NMOSFET **75** is controlled by an ESD trigger and bias circuit **85**. A diode **90** has an anode connected to supply voltage V_{DDH} **55** and a cathode connected to ESD bus **80**. A diode **95** has an anode connected to supply voltage V_{DDL} and a cathode connected to ESD Bus **70**. During an ESD event coupled through either V_{DDH} or V_{DDL} referenced to V_{SS}, diode **90** or diode **95** will forward bias, raising the potential of ESD Bus **80**. ESD trigger and bias circuit **85** senses the transient and biases clamp transistors **70** and **75** into a conductive state to dissipate current from ESD Bus **80** to V_{SS} **65**.

It is assumed that V_{DDL} represents the semiconductor process maximum specified power supply voltage for

NMOSFETs **70** and **75**. This assumption implies that no voltage in excess of V_{DDL} may be applied across the gate oxide of either NMOSFET in normal operation. The NMOSFETs **70** and **75** are stacked in order that the clamp circuit may protect a power supply rail with voltage greater than V_{DDL} by stepping this voltage across two gate oxides. With proper bias conditions on these stacked NMOSFETs, V_{DDH} may operate at twice V_{DDL} without exceeding the gate oxide voltage limit on either NMOSFET **70** or **75**. Under normal IC operation, the ESD Bus **80** will eventually charge up to the potential of V_{DDH} **55**. With the ESD Bus voltage as high as twice V_{DDL}, the series combination of NMOSFETs **70** and **75** must remain nonconductive with no more than V_{DDL} applied across either NMOSFET gate oxide. To achieve this, the ESD trigger and bias circuit **85** must bias the gate of NMOSFET **70** to a voltage intermediate between V_{DDH} and V_{DDL}, and bias the gate of NMOSFET **75** to V_{SS}.

An issue with the stacked clamp circuit of prior art FIG. **2** is the significant increase in area required to produce ESD performance comparable to the single clamp circuit shown in prior art FIG. **1**. For identically sized devices, the series combination of NMOSFETs **70** and **75** in FIG. **2** obviously produce a higher resistance clamp circuit than the single NMOSFET **25** in FIG. **1**. To achieve ESD performance comparable to the single NMOSFET clamp circuit in FIG. **1**, the series NMOSFETs **70** and **75** must each be sized with a channel width about twice the width of NMOSFET **25**. Therefore, alternate configurations of the stacked clamp circuit, which would allow for smaller sizes of NMOSFETs **70** and **75**, yet provide comparable ESD protection, would be desirable.

A limitation with the stacked clamp circuit of prior art FIG. **2** is that the series NMOSFETs **70** and **75** must be sized to protect the most ESD sensitive elements on the IC, whether they are served by the V_{DDL} or V_{DDH} power supply rails. However, in many ICs with multiple power supply voltages, the elements which are served by the V_{DDL} power supply rail are more sensitive to ESD damage than elements served by the V_{DDH} power supply rail. In the clamp circuit of prior art FIG. **2**, stacked NMOSFETs **70** and **75** are sized to protect V_{DDL} for positive ESD events referenced to V_{SS} even though a less resistive single NMOSFET could be used as the primary ESD current dissipation device for ESD events coupled through this lower voltage power supply. Elements on the IC which are served by the V_{DDH} power rail, and assumed less susceptible to ESD damage, could be adequately protected by stacked NMOSFETs of smaller channel width. Accordingly, a need exists for a stacked active MOSFET ESD clamp circuit which retains the advantages of series NMOSFETs to protect a higher voltage power rail, while providing a single NMOSFET as the primary ESD current dissipation device for protecting a lower voltage power rail.

Yet another limitation with the clamp circuit taught by U.S. Pat. No. 5,654,862 is associated with the biasing of the clamp transistors themselves as can be readily seen from FIG. **5** therein. Although an ESD trigger and bias circuit (transistors 552, 560, 561 and resistor 550 of FIG. 5 in U.S. Pat. No. 5,654,862) makes each of two clamp transistors (**501**, **502**) conductive at the same time, the two clamp transistors are not made equally conductive due to differing gate-to-body voltage potentials. During an ESD event, transistor **501** has the full voltage difference between V_{ESD} and V_{SS} applied across its gate and body terminals, whereas transistor **502** has a smaller voltage difference applied across its gate and body terminals. As a result, during an ESD event, one clamp transistor is significantly more conductive than the other series-connected clamp transistor, resulting in significantly increased overall clamp resistance. Accordingly, a need exists for an improved bias network for a stacked active MOSFET ESD clamp circuit.

Thus, a need exists for improved ESD protection that alleviates the problems in the prior art as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of preferred embodiments is considered in conjunction with the following drawings, in which:

FIG. **1** depicts a schematic diagram of a prior art active MOSFET ESD clamp circuit;

FIG. **2** depicts a partial schematic diagram of a prior art stacked active MOSFET ESD clamp circuit;

FIG. **3** depicts a schematic diagram of a first embodiment of the ESD protection circuit in accordance with the present invention;

FIG. **4** depicts a schematic diagram of a second embodiment of the ESD protection circuit in accordance with the present invention;

FIG. **5** depicts a graphical view of the change in nodal voltages of the circuit in FIG. **4** during an ESD event;

FIG. **6** depicts a schematic diagram of a third embodiment of the ESD protection circuit in accordance with the present invention;

FIG. **7** depicts a schematic diagram of a fourth embodiment of the ESD protection circuit in accordance with the present invention;

FIG. **8** depicts a schematic diagram of a first embodiment of a stacked ESD protection circuit in accordance with the present invention; and

FIG. **9** depicts a schematic diagram of a second embodiment of a stacked ESD protection circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

While several embodiments of the present invention will be described in detail below, the present invention includes a circuit providing electrostatic discharge (ESD) protection for internal elements in an integrated circuit (IC) during an ESD event. The circuit has a shunt device, a trigger circuit, and a separate RC delay circuit. The shunting device is connected between two IC power supply rails, and provides the primary current path for a positive ESD event referenced from one power supply rail to the other. The trigger circuit is connected to the shunt device and initially activates the shunt device into a low resistance conductive state in response to an ESD event. The RC delay circuit is also connected to the shunt device and serves to maintain the shunt device in the conductive state, initially produced by the trigger circuit, for the remaining duration of the ESD event. The large area capacitor required to achieve the delay time in this RC circuit may be eliminated by utilizing the gate-to-body capacitance in the existing shunt device. This component elimination offers significant advantages for reduction in the overall clamp circuit area. The embodiments of the present invention will now be described in detail with reference to FIGS. **3–9**.

FIG. **3** depicts a schematic diagram of a first embodiment of the ESD protection circuit of the present invention, a RC triggered/RC delay active MOSFET ESD clamp circuit **100**.

The clamp circuit **100** in FIG. **3** provides IC protection from positive ESD events coupled through a V_{DD} power supply rail **105** to a grounded V_{SS} rail **110**. Likewise, clamp circuit **100** provides protection from negative ESD events coupled through a V_{SS} supply rail to a grounded V_{DD} power supply rail. Those skilled in the art will recognize that the active MOSFET rail clamp circuit **100** may also provide ESD protection for input/output (I/O) pads (not shown) which are served by the supply rails **105** and **110**. The I/O pads are typically coupled to the supply rails via diodes, which may be parasitic elements of the existing output buffer transistors, or intentionally placed for ESD protection.

Clamp circuit **100** in FIG. **3** employs a large NMOSFET transistor **135**, a RC trigger circuit **125**, and a separate RC delay circuit **130**. NMOSFET **135** typically has a source and body terminal connected to V_{SS}, a drain terminal connected to V_{DD}, and a gate terminal connected to the RC trigger circuit **125** and RC delay circuit **130**. As in prior art active MOSFET rail clamp circuits, the performance of clamp circuit **100** will depend primarily on the channel width of NMOSFET **135**. In a representative 0.5 micrometer semiconductor process technology, NMOSFET **135** may, for example, be sized with a channel width of 3,000 micrometers and a channel length of 0.5 micrometer. With the clamp circuit performance largely set by the size of NMOSFET **135**, the most area efficient clamp circuit will be one in which the trigger and delay functions occupy the minimum possible area. The maximum possible percentage of overall clamp area should be allocated for NMOSFET **135**, the primary ESD current dissipation device. As will be explained below, one aspect of the present invention improves on the prior art by reducing the area occupied by the trigger and delay functions, thereby maximizing the clamp circuit ESD performance per area utilized.

Trigger circuit **125** in FIG. **3** is responsible for initially activating NMOSFET **135** into a low resistance conductive state in response to an ESD event. The trigger circuit employs a resistive device **126**, a capacitive device **127**, and a PMOSFET transistor **128**. Resistive device **126** and capacitive device **127** form a RC transient detector **136** with an output **129** connected to the gate of PMOSFET **128**. A first terminal of resistor **126** is connected to V_{DD}. A second terminal of resistor **126** is connected to a first electrode of capacitor **127** at output **129**. A second electrode of capacitor **127** is connected to V_{SS}. The drain of PMOSFET **128** is connected to the gate of NMOSFET **135**, while the source and body are connected to the V_{DD} supply rail **105**. In response to an ESD event that induces a rapid positive voltage transient on the V_{DD} supply rail **105**, trigger circuit **125** initially holds node **129** well below V_{DD}. PMOSFET **128** has a gate connected to node **129**, and turns on and drives the gate of the NMOSFET **135** (node **133**) to the full V_{DD} potential. With the gate terminal at V_{DD}, NMOSFET transistor **135** provides a low resistance shunt between the V_{DD} power supply rail **105** and the V_{SS} power supply rail **110**.

ESD clamp circuit **100** differs from clamp circuit **50** in that trigger circuit **125** need only drive NMOSFET **135** for a period of time comparable to the rise time of the ESD event, rather than the full event duration. The present invention utilizes RC delay circuit **130**, separate from the trigger circuit **125**, to maintain NMOSFET **135** in the low resistance conductive state for the full ESD event duration. As shown in FIG. **3**, the delay circuit **130** employs a resistive device **131** and a capacitive device **132**, each connected between the V_{SS} supply rail **110** and node **133**. During normal operation of the IC, with constant V_{DD} power supply level, trigger circuit **136** remains inactive and resistive device **131** ensures NMOSFET **135** is biased in the nonconductive state. During an ESD event which enables trigger circuit **125**, node **133** which is connected to the gate of NMOSFET **135**, will be driven to the full V_{DD} voltage. After an interval set by the RC trigger circuit **125** time constant, PMOSFET **128** turns off, isolating node **133** from the V_{DD} supply rail. The voltage at node **133** will then decay to V_{SS} with a characteristic time constant set by the product of the net capacitance between node **133** and V_{SS} and the resistance of resistive device **131**. In a preferred form, capacitive device **132** actually represents the parasitic gate-to-body capacitance in NMOSFET **135**. Since NMOSFET **135** must be sized quite large to produce the desired ESD protection, the gate electrode of this device provides considerable capacitance to V_{SS}. An additional capacitive device, separate from NMOSFET **135**, is typically not needed to achieve the required RC time delay. This arrangement offers significant advantages. NMOSFET **135** may now serve two functions. Firstly, NMOSFET **135** serves as the primary ESD current dissipation device, sized as required to achieve robust ESD performance. Secondly, NMOSFET **135** now provides a convenient large capacitance to V_{SS} which may be advantageously utilized to obtain the conductive mode delay function required of the clamp circuit. No other large area capacitive device is needed to achieve this delay. Therefore, by separating the trigger and delay functions, the ESD current dissipation device (NMOSFET **135**) can now be utilized as an area efficient mechanism to achieve the clamp delay function. This feature is a significant improvement over the prior art, where combined trigger and delay functions necessitate a RC circuit of much larger area.

FIG. **4** depicts a schematic diagram of a second embodiment of the ESD protection circuit of the present invention. The clamp circuit **140** in FIG. **4** differs from the clamp circuit **100** in FIG. **3** only in a RC trigger circuit **175**. The RC transient detector **136** from FIG. **3** is inverted so that a capacitive device **176** is connected to a power supply rail V_{DD} **145**, while a resistive device **177** is connected to a power supply rail V_{SS} **150**. Capacitive device **176** is connected in series with resistive device **177**. In addition, an inverter stage, consisting of a PMOSFET **179** and a NMOSFET **180** which are connected in series between supply rail V_{DD} and supply rail V_{SS}, has been added between a RC transient detector **183** and a PMOSFET **182**. It should be assumed that a RC delay circuit **190** of FIG. **4** is equivalent to RC delay circuit **130** of FIG. **3**. In a preferred form, a capacitive device **192** in RC delay circuit **190** is assumed to represent the parasitic gate-to-body capacitance of a NMOSFET **195**. During normal operation of the IC, NMOSFET **195** is biased in the nonconductive state. Those skilled in the art will recognize that alternate configurations of the trigger circuits **125** and **175** are possible, utilizing additional inverter stages and alternate RC transient detector circuits.

The operation of clamp circuit **140** during an ESD event can be explained with the aid of FIG. **5**. In FIG. **5**, the results of a circuit simulation of clamp circuit **140** in FIG. **4** is shown. A Human Body Model (HBM) ESD pulse with a peak amplitude of 4,000 volts is applied to the V_{DD} rail **145**, with respect to grounded V_{SS} rail **150**. The variation of nodal voltages during the first 250 nanoseconds of the ESD event are shown. For the simulation, NMOSFET **195** is sized having width/length dimensions equal to 3000/0.5 micrometers, respectively. PMOSFET **182**, PMOSFET **179**, and NMOSFET **180** are sized at 300/0.5 micrometers, 40/0.5 micrometers, and 20/0.5 micrometers, respectively. The time constant of RC transient detector **183** is set to about 20

nanoseconds. The time constant of the RC delay circuit **190** is set to about 1,000 nanoseconds. As shown in FIG. **5**, the HBM pulse is applied to the clamp circuit at 50 nanoseconds. The V_{DD} rail voltage is seen to rise quickly to a peak of 5.8 volts in about 8 nanoseconds, and then decay to V_{SS} over a period of about 500 nanoseconds. The HBM current waveform (not shown) exhibits a similar shape, with a peak current of about 2.7 amperes. During the HBM ESD event, the RC transient detector node **178** rises initially with V_{DD} to about 3.7 volts but falls quickly due to the short time constant for this RC network. Node **181**, which represents the output of the PMOSFET **179**/NMOSFET **180** inverter, is initially low but transitions high as the RC transient detector **183** times out. PMOSFET **182**, with its gate connected to node **181**, is therefore biased into saturation initially, maintaining node **194** at V_{DD}. About 20 nanoseconds into the HBM event, PMOSFET **182** is turned off, effectively isolating node **194** from V_{DD}. At this point, resistive device **191** is left to pull the gate of NMOSFET **195** (node **194**) down to V_{SS}. The time required to turn off NMOSFET **195** is dependent on the total capacitance at node **194** to V_{SS}, and the resistance of resistive device **191**. Note that in the initial stages of the ESD event, V_{DD} and the gate of NMOSFET **195** are at the same potential, indicating proper operation of the RC trigger circuit **175**. But, after PMOSFET **182** shuts off, the NMOSFET gate voltage decays to V_{SS} at a rate slower than the decay time of V_{DD}. Therefore, in the time interval after trigger circuit **175** times out, the NMOSFET **195** gate voltage exceeds the V_{DD} voltage. This bias condition for NMOSFET **195** results in a more rapid drop in the V_{DD} rail potential than would occur if the gate voltage directly tracked V_{DD}. This is a fundamental difference in the clamp circuit operation, as compared to the prior art clamp circuit of FIG. **1**. In the prior art clamp circuit of FIG. **1**, the NMOSFET **25** gate voltage will follow the V_{DD} rail voltage throughout the ESD event. The time constant of the RC trigger circuit in FIG. **4** should be set to equal or just exceed the HBM pulse rise time. With this timing, the NMOSFET **195** gate is isolated from the V_{DD} power rail at or near the peak V_{DD} resulting from the ESD event. As the HBM pulse is dissipated, the NMOSFET **195** gate is held above the V_{DD} rail, resulting in a less resistive, more efficient clamp circuit.

ESD clamp circuit **100** in FIG. **3** and clamp circuit **140** in FIG. **4** differ from the clamp circuit **50** of FIG. **1** in that the RC trigger circuit need only drive the large dissipation NMOSFET for a period of time comparable to the rise time of the HBM ESD event, rather than the full event duration. In the prior art clamp circuit in FIG. **1**, the trigger circuit must be sized to achieve a RC time constant of at least 200 nanoseconds. In actual practice, trigger circuits with time constants of up to 1,000 nanoseconds are often used. In the present invention, clamp circuit **100** and clamp circuit **140**, each require a trigger circuit sized to achieve a RC time constant of only about 20 nanoseconds. Therefore the trigger circuit in the present invention requires only about ten percent of the layout area of the smallest possible trigger circuit in the prior art clamp circuit **50**. As mentioned previously, the area utilized by trigger circuit **15** in prior art FIG. **1** commonly represents twenty to fifty percent of the area required for the large ESD current dissipation device. With the clamp circuit performance largely set by the size of this NMOSFET, the most area efficient clamp circuit will be one in which the trigger and delay functions occupy the minimum possible area. Therefore, the present invention improves on the prior art by reducing the area occupied by the trigger and delay functions, thereby maximizing the clamp circuit ESD performance per area utilized.

The two embodiments of the present invention shown in FIG. **3** and FIG. **4** are also superior to the prior art in that they are less susceptible to false triggering during normal ramp up of the V_{DD} power supply. All RC triggered clamp circuits are at risk in IC applications where the V_{DD} power supply ramp-up time is on the order of the trigger circuit RC time constant. As described earlier, the RC trigger circuit in the prior art FIG. **1** requires a time constant of at least 200 nanoseconds. The RC trigger circuits illustrated in two embodiments of the present invention (FIG. **3** and FIG. **4**) require a time constant of only about 20 nanoseconds. This translates into at least an order of magnitude improvement in the maximum tolerable power supply ramp-up rate.

FIG. **6** depicts a schematic diagram of a third embodiment of the ESD protection circuit in accordance with the present invention. A clamp circuit **200** in FIG. **6** differs from the previous clamp circuits **100** and **140** in that the primary ESD current dissipation device is now a PMOSFET transistor. The RC trigger circuit and the RC delay circuit have been modified to control this PMOSFET shunting device. Clamp circuit **200** in FIG. **6** employs a large PMOSFET transistor **235**, a RC trigger circuit **225**, and a separate RC delay circuit **230**. PMOSFET **235** typically has a source and body terminal connected to V_{DD} **205**, a drain terminal connected to V_{SS} **210**, and a gate terminal connected to the RC trigger circuit **225** and RC delay circuit **230**.

Trigger circuit **225** in FIG. **6** initially activates PMOSFET **235** into a low resistance, conductive state in response to an ESD event. The trigger circuit employs a resistive device **226**, a capacitive device **227**, and a NMOSFET transistor **228**. Resistive device **226** and capacitive device **227** are connected in series between supply rails V_{DD} and V_{SS} and form a RC transient detector with an output **229** connected to the gate of NMOSFET **228**. A drain of NMOSFET **228** is connected to the gate of PMOSFET **235**, while the source and body thereof are connected to the V_{SS} supply rail **210**. In response to an ESD event that induces a rapid positive voltage transient on the V_{DD} rail **205**, trigger circuit **225** initially pulls node **229** to near V_{DD}. NMOSFET **228**, with its gate connected to node **229**, turns on and drives the gate of PMOSFET **235** (node **233**) to the supply rail V_{SS} potential. Once turned on, PMOSFET transistor **235** provides a low resistance shunt between the V_{DD} supply rail **205** and the V_{SS} supply rail **210**. RC delay circuit **230** maintains the shunt device in the conductive state, initially produced by the trigger circuit, for the remaining duration of the ESD event. As shown in FIG. **6**, the delay circuit **230** employs a resistive device **231** and capacitive device **232**, with both devices connected between node **233** and the VDD rail **205**. During an ESD event which enables RC trigger circuit **225**, node **233**, connected to the gate of PMOSFET **235**, will be driven to V_{SS}. After an interval set by the RC trigger circuit time constant, NMOSFET **228** turns off, isolating node **233** from the V_{SS} supply rail **210**. The voltage at node **233** will then rise to V_{DD} with a characteristic time constant set by the product of the net capacitance between node **233** and V_{DD} and the resistance of resistive device **231**. In a preferred form of circuit **200**, capacitive device **232** actually represents the parasitic gate-to-body capacitance in PMOSFET **235**. As before, this arrangement offers significant area savings and performance advantages. During normal operation of the IC, with constant V_{DD} power supply level, PMOSFET **235** is biased in the nonconductive state.

A fundamental difference in the present invention and the prior art circuit **50** is the separation of the RC trigger and RC delay circuits which drive the gate of the large ESD current dissipation MOSFET. The prior art ESD clamp circuit of

FIG. **1** utilizes a single RC circuit **15** to both respond to an ESD event (trigger function) and to maintain the large MOSFET in the conductive mode for the full event duration (delay function). With this approach, a large RC circuit is required to protect for a HBM ESD event of a few hundred nanoseconds duration. By separating the trigger and delay functions, the circuit of the present invention can achieve the required RC delay function by utilizing the existing gate capacitance provided by the large ESD current dissipation MOSFET. This provides for significant savings in the overall clamp circuit area.

A notable feature of the present invention is the compact RC delay circuit separate from the trigger circuit. This RC delay circuit greatly reduces the demands on the trigger portion of the circuit. The trigger circuitry now need only fully charge the large MOSFET gate before timing out, rather than remain active throughout the ESD event. These reduced demands on the trigger circuit greatly simplify the problem of designing alternate trigger circuits. In fact, with the separate RC delay circuit, it is possible to design a robust voltage threshold triggered active MOSFET ESD clamp circuit.

In certain IC applications, a voltage threshold triggered ESD clamp circuit offers clear advantages over a RC (transient) triggered clamp circuit. Such a clamp circuit protecting a V_{DD} power rail would be essentially immune to false triggering during a very fast ramp-up of the V_{DD} power supply. This advantage may be essential in certain battery powered and "hot plugged" IC applications. In addition, a threshold triggered clamp circuit could be used to protect other circuit nodes which see rapid signal transitions during normal IC operation. A RC transient triggered clamp circuit may be unusable in this application.

FIG. **7** is a schematic view of a fourth embodiment of the ESD protection circuit of the present invention. In FIG. **7**, the RC trigger circuit of the previous embodiments has been replaced by a voltage sensing trigger circuit. However, the separate RC delay circuit key to the previous embodiments is retained. Therefore, circuit **300** in FIG. **7** represents a threshold triggered/RC delay active MOSFET ESD clamp circuit. This embodiment still maintains the size advantage of the previous embodiments and only differs in the manner in which the clamp circuit is initially triggered into the conductive mode. A threshold trigger circuit **325** in FIG. **7** initially activates a NMOSFET **345** into a low resistance conductive state in response to an ESD event which elevates a V_{DD} power supply rail **305** above a predetermined voltage threshold. The trigger circuit employs a diode string, two resistive devices, a NMOSFET and a PMOSFET transistor. A diode string **327** is placed between the V_{DD} power supply rail **305** and a node **328**, with the anode of the first diode in the string connected to the V_{DD} power supply rail, and the cathode of the last diode in the string connected to node **328**. A resistive device **326** is connected between node **328** and the V_{SS} power supply rail **310**. Node **328** is also connected to the gate of a NMOSFET transistor **329**. A source and body of NMOSFET **329** are connected to the V_{SS} power supply rail **310**, and the drain is connected to a node **331**. A resistive device **330** is connected between node **331** and the V_{DD} power supply rail **305**. Also connected to node **331** is the gate of a PMOSFET **332**. A source and body of PMOSFET **332** are connected to the V_{DD} power supply rail **305**, and the drain is connected to a node **344**, which is connected to a gate of a large NMOSFET **345**. A RC delay circuit **340** having a parallel-connected capacitive device **342** and a resistive device **341** between node **344** and power supply rail V_{SS} provides the same function as described for circuit **140** in FIG. **4**.

The number of diodes in string **327** is preferably adjusted such that the V_{DD} power supply rail **305** must reach a predetermined voltage level above a normal supply voltage value before the threshold trigger circuit becomes active. With the V_{DD} power supply rail **305** below this threshold, NMOSFET **329** and PMOSFET **332** are biased in the nonconductive state, and the clamp circuit remains inactive. In response to an ESD event that induces a positive voltage transient on the V_{DD} power supply rail **305**, node **328** will remain near V_{SS} until the V_{DD} power supply rail voltage exceeds the sum of the forward bias voltage drops in diode string **327**. Above this threshold, the diode string becomes conductive, elevating node **328** as current flows through resistive device **326** to V_{SS}. Resistive devices **326** and **330** are both typically sized to achieve a resistance of a few thousand ohms. NMOSFET **329** turns on when the voltage at node **328** exceeds the NMOSFET threshold voltage. As NMOSFET **329** turns on, node **331** is pulled toward the V_{SS} power supply rail potential. PMOSFET **332**, with its gate now held to near V_{SS}, drives the gate of the large NMOSFET **345** to the full V_{DD} potential. Once turned on, NMOSFET transistor **345** provides a low resistance shunt between the V_{DD} power supply rail **305** and the V_{SS} power supply rail **310**. As the ESD event is dissipated, the V_{DD} rail voltage will drop below the threshold voltage of trigger circuit **325**. At this point, diode string **327** ceases forward biased conduction, and resistive device **326** pulls node **328** to V_{SS}. With node **328** at V_{SS}, NMOSFET **329** turns off, allowing resistive device **330** to pull node **331** to V_{DD}. With node **331** at V_{DD}, PMOSFET **332** turns off, isolating the gate of NMOSFET **345** (node **344**) from the V_{DD} power supply rail **305**. At this point, the RC delay circuit **340** controls the rate at which the voltage on node **344** decays to V_{SS}. RC delay circuit **340** operates in a manner similar to that previously described for RC delay circuit **130** of FIG. **3**.

It is very difficult to design an efficient, stable threshold-triggered active MOSFET ESD clamp circuit without an added RC delay function. The problem is due to the dual requirements of a high trigger voltage, and strong gate drive for the large NMOSFET for the duration of the ESD event. In response to a positive ESD event coupled through the V_{DD} power supply rail, it is preferable to electrically short-circuit V_{DD} to V_{SS} when the trigger threshold is reached, and to maintain the short-circuit for a period of time until the ESD event is completely dissipated. A simple threshold clamp with no built-in delay function would turn off as soon as V_{DD} dropped below the trigger threshold. The V_{DD} rail would then rapidly rise again as the IC shared charge with the large capacitance of the ESD source. The threshold clamp would then turn on again and the process would repeat over and over until the ESD source was discharged to near the trigger level. These problems are avoided with the voltage threshold triggered/RC delay active MOSFET clamp circuit as depicted in FIG. **7**.

Those skilled in the art will recognize that numerous alternate configurations of the threshold trigger circuit **325** may be utilized without deviating from the scope and spirit of this invention.

FIG. **8** is a schematic view of a first embodiment of a multiple power supply stacked ESD clamp circuit in accordance with the present invention. A stacked clamp circuit **400** in FIG. **8** provides ESD protection for ICs which allow voltages in excess of the internal power supply voltage for a specified baseline process technology to be brought on board the IC. Protection for this higher voltage power rail can be achieved with stacked, or series-connected active MOSFET clamp circuits. With minor modifications, circuit

400 is formed by vertically stacking two single power supply active MOSFET rail clamp circuits from FIG. 3. Circuit 400 is therefore a stacked RC triggered/RC delay active MOSFET clamp circuit. In FIG. 8, three power supply rails are shown and labeled V_{DDH} 405, V_{DDL} 410, and V_{SS} 415. It is assumed that supply rail V_{DDL} represents the maximum specified power supply voltage for a semiconductor process for all MOSFETs in the clamp circuit. This limit implies that no voltage in excess of V_{DDL} may be applied across the gate oxide of any MOSFET in normal operation. It is further assumed that power supply rail V_{DDH} may, under normal operation, be maintained at a voltage up to twice V_{DDL}. In a typical IC application, V_{DDL} and V_{DDH} may, for example, reach maximum voltages of 3.6 volts and 5.5 volts, respectively.

Clamp circuit 400 in FIG. 8 employs a large NMOSFET transistor 435, a RC trigger circuit 425, and a separate RC delay circuit 430 to provide ESD protection between power supply rails V_{DDH} and V_{DDL}. NMOSFET 435 has a drain connected to V_{DDH} 405, a source connected to V_{DDL} 410, a body connected to V_{SS} 415, and a gate connected to both a RC trigger circuit 425 and a RC delay circuit 430. NMOSFET 435 serves as the primary ESD current dissipation device between V_{DDH} and V_{DDL} . Similarly, for ESD protection between power supply rails V_{DDL} and V_{SS}, clamp circuit 400 employs a large NMOSFET transistor 465, a RC trigger circuit 450, and a separate RC delay circuit 460. NMOSFET 465, with a drain connected to V_{DDL} 410, a body and a source connected to V_{SS} 415, and a gate connected to both a RC trigger circuit 450 and a RC delay circuit 460, serves as the primary ESD current dissipation device between V_{DDL} and V_{SS}. Clamp circuit 400 provides IC protection from positive ESD events coupled through the V_{DDH} power supply rail 405 to either a grounded V_{DDL} rail 410 (via NMOSFET 435) or a grounded V_{SS} rail 415 (via the series combination of NMOSFET 435 and NMOSFET 465). In addition, clamp circuit 400 provides IC protection from positive ESD events coupled through the V_{DDL} power supply rail 410 to a grounded V_{SS} rail 415 (via NMOSFET 465). In contrast to the prior art stacked clamp circuit shown in FIG. 2, V_{DDL} to V_{SS} protection is provided via a single NMOSFET 465, rather than stacked NMOSFETs. In many ICs with multiple power supply voltages, internal elements which are served by the V_{DDL} power supply rail are more sensitive to ESD damage than elements served by the higher voltage V_{DDH} power supply rail. The stacked clamp circuit in FIG. 8 provides an efficient clamp network in these applications. Elements on the IC which are served by the V_{DDL} power supply rail, and assumed more susceptible to ESD damage, are protected by the single NMOSFET 465. Stacked NMOSFETs 435 and 465 may now be sized to protect the more ESD resistant elements served by the V_{DDH} power supply rail. Therefore, a stack of smaller-sized NMOSFETs may be utilized than required in the prior art circuit of FIG. 2. It should be apparent that the stacked active MOSFET rail clamp circuit 400 may also provide ESD protection for input/output (I/O) pads (not shown) which are served by the power supply rails 405, 410 and 415. The I/O pads are typically coupled to the supply rails via diodes, which may be parasitic elements of the existing output buffer transistors, or intentionally placed for ESD protection.

The operation of stacked clamp circuit 400 in FIG. 8 depends on whether the ESD event is coupled through the V_{DDH} or V_{DDL} power supply rails. In response to a positive ESD event coupled through the V_{DDH} power rail, trigger circuit 425 initially activates both NMOSFET 435 and NMOSFET 465 into a low resistance conductive state. The trigger circuit employs a resistive device 426, a capacitive device 427, and PMOSFET transistors 428 and 475. Resistive device 426 and capacitive device 427 form a RC transient detector with an output 429 connected to a gate of a PMOSFET 428. A drain of PMOSFET 428 is connected to a gate of NMOSFET 435, while the source and body thereof are connected to the V_{DDH} rail 405. PMOSFET 475, not used in the single supply clamp circuits 100 and 140, allows trigger circuit 425 to drive a gate of NMOSFET 465. A drain and body of PMOSFET 475 is connected to a node 433. A source of PMOSFET 475 is connected to a node 463, and a gate thereof is connected to V_{DDL}. In response to an ESD event that induces a rapid positive voltage transient on the V_{DDH} power supply rail 405, trigger circuit 425 initially holds node 429 well below V_{DDH}. PMOSFET 428 turns on and drives the gate of NMOSFET 435 (node 433) to the full V_{DDH} potential. As the potential at node 433 rises, PMOSFET 475, with its gate connected to V_{DDL}, turns on and drives the gate of NMOSFET 465 to V_{DDH}. NMOSFETs 435 and 465, each with its respective body at V_{SS} and gate at V_{DD}, provide a low resistance shunt between the V_{DDH} power supply rail 405 and the V_{SS} power supply rail 415. Capacitance between V_{DDL} and V_{SS}, distributed throughout the IC, serves to ensure the gate of PMOSFET 475 is initially held below node 433. Diode 454 in the lower clamp trigger circuit 450 acts as a current blocking device to prevent charge from leaving the gate of NMOSFET 465 and therefore keep the potential of the gate of NMOSFET 465 close to the V_{DDH} potential. Therefore, NMOSFET 465 is guaranteed to be biased on strongly and maintain a low resistance. Without diode 454, a leakage path could exist through the parasitic diode in PMOSFET 453 to the V_{DDL} rail.

RC trigger circuit 425 need only drive NMOSFETs 435 and 465 for a period of time comparable to the rise time of the ESD event, rather than the full event duration. RC delay circuits 430 and 460, separate from trigger circuit 425, maintain NMOSFETs 435 and 465 in the low resistance conductive state for the full remaining ESD event duration. As shown in FIG. 8, RC delay circuit 430 employs a resistive device 431 connected between the V_{DDL} power supply rail 410 and node 433, and a capacitive device 432 connected between the V_{SS} power supply rail 415 and node 433. In a similar manner, RC delay circuit 460 employs a resistive device 461 and a capacitive device 462, each connected between the V_{SS} rail 415 and node 463. In a preferred form, each capacitive device 432 and 462 is respectively assumed to represent the parasitic gate-to-body capacitance of NMOSFETs 435 and 465.

During normal operation of the IC, with constant V_{DDH} and V_{DDL} power supply levels, trigger circuit 425 remains inactive and resistive device 461 will hold the gate of NMOSFET 465 to V_{SS}. In addition, resistive device 431 will hold the gate of NMOSFET 435 to V_{DDL}. With its body at V_{SS}, and both the gate and source at the V_{DDL} potential, NMOSFET 435 will not conduct MOSFET current. Note that, under normal V_{DDL} and V_{DDH} bias conditions, no MOSFET in stacked clamp circuit 400 has a voltage in excess of V_{DDL} across the gate oxide.

During an ESD event which enables trigger circuit 425, node 433, connected to the gate of NMOSFET 135, will be driven to the full V_{DD} voltage. After an interval set by the RC trigger circuit 425 time constant, PMOSFET 428 turns off, isolating nodes 433 and 463 from the V_{DDH} power supply rail. The voltage at nodes 433 and 463 will then decay to V_{SS} with characteristic time constants set by RC delay circuits 430 and 460, respectively. In a preferred

embodiment, rather than representing separate elements in the stacked clamp circuit, capacitive devices **432** and **462** actually represent the parasitic gate-to-body capacitances in NMOSFET **435** and **465**, respectively. As in the previous embodiments of this invention, this arrangement allows for significant space savings in the stacked clamp circuit.

In response to positive ESD events coupled through the V_{DDL} power supply rail **410** to the grounded V_{SS} power supply rail **415**, RC trigger circuit **450**, RC delay circuit **460**, and NMOSFET **465** each function as in clamp circuit **100** in FIG. **3**. Trigger circuit **450** is slightly modified with the addition of diode **454**, placed between V_{DDL} and PMOSFET **453**. As explained above, this diode is only needed during ESD events coupled through the V_{DDH} rail. For ESD events coupled through the V_{DDL} power supply rail, this diode does prevent trigger circuit **450** from driving the gate of NMOSFET **465** to the full V_{DDL} potential. This causes a small reduction in lower clamp performance as compared to circuit **100** in FIG. **3**.

A key element of this invention is the utilization of PMOSFET **475** to pull the gate of NMOSFET **465** up to the full V_{DDH} potential for ESD events coupled through the V_{DDH} power supply rail. Consider the operation of stacked clamp circuit **400** without including PMOSFET **475** and diode **454**. Without these two devices, the circuit would resemble two clamp circuits **100** from FIG. **3** stacked vertically. During a positive ESD event coupled through V_{DDH}, the gate of NMOSFET **435** would be pulled to the full V_{DDH}. The gate of NMOSFET **465**, however, would only be pulled to V_{DDL}. Therefore, with reduced gate-to-body voltage differential, NMOSFET **465** would form a more resistive ESD current dissipation device than NMOSFET **435**. This would reduce the overall stacked clamp circuit performance. The "gate boost" provided to NMOSFET **465** by PMOSFET **475** is needed to ensure that the full ESD voltage across the stacked rail clamp circuit is applied across the gate-to-body terminals of both seriesconnected NMOSFETs. This represents a significant improvement over the circuit taught in the prior art.

FIG. **9** is a schematic view of a second embodiment of a multiple power supply stacked ESD clamp circuit in accordance with the present invention. Stacked clamp circuit **500** in FIG. **9** is intended for those applications where ESD protection is needed for the V_{DDH} power supply rail only. With this embodiment, protection for the V_{DDL} power supply rail must be provided elsewhere. Note that in circuit **500**, the lower RC trigger circuit **450** of FIG. **8** has been removed. Also note that the V_{DDL} power supply rail **510** need not be connected between NMOSFETs **535** and **565**, but could be so connected. Therefore, with no need for an intermediate connection to V_{DDL}, NMOSFETs **535** and **565** may be easily drawn on silicon in the same active opening utilizing adjacent gates for the two transistors. This feature may provide a more compact layout. Connection to V_{DDL} is required elsewhere in circuit **500** in order to provide proper bias conditions during normal circuit operation.

It is understood that additional embodiments may also be formed that fall within the scope of the present invention as claimed below. Although the invention has been described and illustrated with reference to specific embodiments, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that modifications and variations may be made without departing from the spirit and scope of the invention. Therefore, it is intended that this invention encompasses all the variations and modifications as fall within the scope of the appended claims.

We claim:

1. A circuit for providing electrostatic discharge (ESD) protection for internal elements in an integrated circuit during an ESD event, the circuit comprising:

a shunting device coupled to a first power supply rail for receiving a first voltage and coupled to a second power supply rail for receiving a second voltage, said shunting device providing a primary current path for a positive ESD event occurring between the first and second power supply rails;

a triggering means coupled to the shunting device, the triggering means initially activating the shunting device into a low resistance conductive state in response to the positive ESD event, the triggering means maintains the shunting device in the low resistance conductive state for a first period of time; and

a delay means connected to the shunting device, the delay means having a circuit portion which uses both resistance and capacitance to maintain the shunting device in the conductive state for a second period of time, at least a portion of the second period of time being subsequent to the first period of time and continuing at least until substantial conclusion of detrimental ESD voltage.

2. The circuit of claim **1** wherein the first power supply rail is a V_{DD} power supply rail, and the second power supply rail is a V_{SS} power supply rail, wherein V_{DD} is more positive than V_{SS} under normal operating conditions.

3. The circuit of claim **1** wherein the shunting device further comprises a MOSFET transistor having a gate and body, and first and second current conducting electrodes.

4. The circuit of claim **3** wherein the delay means comprises:

a resistive device having a first terminal coupled to the gate of the MOSFET transistor and a second terminal coupled to the second power supply rail; and

a capacitor having a first electrode coupled to the gate of the MOSFET transistor and the first terminal of the resistive device, the capacitor having a second electrode coupled to the second power supply rail.

5. The circuit of claim **1** wherein the capacitance of the circuit portion of the delay means comprises a parasitic capacitance between the gate and body of the MOSFET transistor without implementing a discrete capacitor.

6. The circuit of claim **1** wherein the triggering means further comprises one of a resistor and capacitor (RC) circuit or a voltage level detector circuit.

7. The circuit of claim **1** wherein the triggering means further comprises:

a first transistor having a current electrode coupled to the first power supply rail, a control electrode, and a second current conducting electrode coupled to the shunting device to control current conduction of the shunting device;

a resistive device having a first terminal coupled to the first power supply rail, and having a second terminal;

a capacitive device having a first electrode coupled to the second terminal of the resistive device, and having a second electrode coupled to the second power supply rail.

8. A circuit for providing electrostatic discharge (ESD) protection for internal elements in an integrated circuit during an ESD event, the circuit comprising:

a shunting means coupled to a first power supply rail for receiving a first voltage and a second power supply rail for receiving a second voltage, said shunting means

providing a primary current path for a positive ESD event occurring between the first and second power supply rails;

a triggering means coupled to the shunting means, the triggering means initially activating the shunting means into a low resistance conductive state in response to the positive ESD event, the triggering means maintaining the shunting means in the low resistance conductive state for a first period of time, the triggering means further comprising:

a first transistor of a first conductivity type having a first current electrode coupled to the first power supply rail, a control electrode, and a second current conducting electrode coupled to the shunting means;

a first resistive device having a first terminal coupled to the first power supply rail, and having a second terminal coupled to the control electrode of the first transistor;

a second transistor of a second conductivity type having a first current electrode coupled to the second terminal of the first resistive device, a control electrode, and a second current conducting electrode coupled to the second power supply rail;

a plurality of series-connected diodes connected between the first power supply rail and the control electrode of the second transistor; and

a second resistive device having a first terminal coupled to the control electrode of the second transistor, and having a second terminal coupled to the second power supply rail; and

a delay means coupled to the shunting means, the delay means having a first resistor and capacitor network which maintains the shunting means in the conductive state for a second period of time which is significantly longer than the first period of time and continues at least until conclusion of detrimental voltages associated with the ESD event.

9. A circuit for providing electrostatic discharge (ESD) protection for internal elements in an integrated circuit during an ESD event, the circuit comprising:

a shunting means coupled to a first power supply rail for receiving a first voltage and a second power supply rail for receiving a second voltage, said shunting means providing a primary current path for a positive ESD event occurring between the first and second power supply rails;

a triggering means coupled to the shunting means, the triggering means initially activating the shunting means into a low resistance conductive state in response to the positive ESD event, the triggering means maintaining high shunting means in the low resistance conductive state for a first period of time, triggering means further comprising:

a first transistor of a first conductivity type having a first current electrode coupled to the first power supply rail, a control electrode, and a second current conducting electrode coupled to the shunting means;

a second transistor of the first conductivity type having a first current electrode coupled to the first power supply rail, a control electrode, and a second current electrode coupled to the control electrode of the first transistor; and

a third transistor of a second conductivity type having a first current electrode coupled to the second current electrode of the second transistor, a control electrode, and a third current conducting electrode coupled to the second power supply rail;

a capacitive device having a first electrode coupled to the first power supply rail, and having a second electrode coupled to the control electrode of each of the second and third transistors; and

a resistive device having a first terminal coupled to the second electrode of the capacitive device, and having a second terminal coupled to the second power supply rail; and

a delay means coupled to the shunting means, the delay means having a first resistor and capacitor network which maintains the shunting means in the conductive state for a second period of time which is significantly longer than the first period of time and continues at least until conclusion of detrimental voltages associated with the ESD event.

10. A circuit for electrostatic discharge protection in an integrated circuit, comprising:

a first current shunting device, the first current shunting device having a first current electrode connected to a first supply voltage conductor for conducting a first operating supply voltage, a second current electrode, and a control electrode;

a second current shunting device, the second current shunting device having a first current electrode connected to the second current electrode of the first current shunting device, a second current electrode connected to a second supply voltage conductor, and a control electrode, the second supply voltage conductor conducting a second operating supply voltage which is less in magnitude than the first operating supply voltage;

a third supply voltage conductor which is electrically connected to both the second current electrode of the first current shunting device and the first current electrode of the second current shunting device, the third supply voltage conductor for conducting a third operating supply voltage which is intermediate in value to the first and second operating supply voltages;

a first trigger circuit coupled to the first and second current shunting devices, the first trigger circuit initially enabling conduction of the first and second current shunting devices in response to an electrostatic discharge event on the first supply voltage conductor;

a first delay circuit coupled to the first current shunting device for maintaining conduction of the first current shunting device until substantial completion of the electrostatic discharge event;

a second trigger circuit coupled to the second current shunting device, the second trigger circuit initially enabling conduction of the second current shunting device in response to an electrostatic discharge event on the third supply voltage conductor; and

a second delay circuit coupled to the second current shunting device for maintaining conduction of the second current shunting device until substantial completion of the electrostatic discharge event.

11. The circuit of claim **10** wherein the first trigger circuit further comprises:

a sensing and bias transistor having a first current electrode coupled to the control electrode of the first current shunting device, a control electrode coupled to the third supply voltage conductor, and a second current electrode coupled to the control electrode of the second current shunting device, the sensing and bias transistor sensing when the control electrode of the first current shunting device exceeds the third operating supply

voltage by a device threshold voltage and in response, becoming conductive to place the first operating supply voltage on both control electrodes of the first and second current shunting devices.

12. The circuit of claim **11** wherein the second trigger circuit further comprises:

a current blocking device coupled to the third supply voltage conductor, the current blocking device preventing charge leakage from the control electrode of the second current shunting device during the electrostatic discharge event in order to maintain the control electrode of the second current shunting device at substantially the first operating supply voltage.

13. circuit of claim **10** wherein the first delay circuit further comprises:

a first resistive device having a first terminal coupled to the control electrode of the first current shunting device, and having a second terminal coupled to the third supply voltage conductor; and

a first capacitor having a first electrode coupled to the control electrode of the first current shunting device and the first terminal of the first resistive device, the first capacitor having a second electrode coupled to a reference conductor; and

wherein the second delay circuit further comprises:

a second resistive device having a first terminal coupled to the control electrode of the second current shunting device, and having a second terminal coupled to the second power supply voltage conductor; and

a second capacitor having a first electrode coupled to both the control electrode of the second current shunting device and the first terminal of the second resistive device, the second capacitor having a second electrode coupled to the second supply voltage conductor.

14. The circuit of claim **13** wherein the first delay circuit and the second delay circuit each further comprises additional parasitic capacitance between a gate and body of the first and second current shunting devices, respectively.

15. A circuit for electrostatic discharge protection in an integrated circuit, comprising:

a first current shunting device, the first current shunting device having a first current electrode connected to a first power supply voltage conductor for conducting a first power supply voltage, a second current electrode, and a control electrode;

a second current shunting device, the second current shunting device having a first current electrode connected to the second current electrode of the first current shunting device, a second current electrode connected to a second power supply voltage conductor for conducting a second power supply voltage, and a control electrode, the second power supply voltage being less in magnitude than the first power supply voltage;

a trigger circuit coupled to the first and second current shunting devices, the trigger circuit initially enabling conduction of the first and second current shunting devices in response to a positive ESD event on the first power supply voltage conductor, the trigger circuit maintaining the first and second current shunting devices in a conductive state for a first period of time;

a first delay circuit having a first RC time constant, the first delay circuit comprising:

a first resistive device having a first terminal coupled to the control electrode of the first current shunting device, and having a second terminal coupled to a third power supply voltage conductor; and

a first parasitic capacitance between the control electrode and body of the first current shunting device; and

a second delay circuit having a second RC time constant, the second delay circuit comprising:

a second resistive device having a first terminal coupled to the control electrode of the second current shunting device, and having a second terminal coupled to the second power supply voltage conductor; and

a second parasitic capacitance between the control electrode and body of the second current shunting device;

wherein the third power supply voltage conductor provides a third power supply voltage which is intermediate the first and second power supply voltages, the third power supply voltage being used to bias the first current shunting device, the trigger circuit and the first delay circuit during a normal mode of operation.

16. The circuit of claim **15** wherein the trigger circuit further comprises:

a sensing and bias device having a first current electrode connected to the control electrode of the first current shunting device, a second current electrode connected to the control electrode of the second current shunting device, and a control electrode connected to the third power supply voltage conductor, the sensing and bias device placing a voltage value substantially equal to the first power supply voltage on the control electrode of each of the first and second current shunting devices during an electrostatic discharge event.

17. The circuit of claim **15** wherein the first delay circuit further comprises:

a first capacitor having a first electrode coupled to both the control electrode of the first current shunting device first terminal of the first resistive device, the first capacitor having a second electrode coupled to a reference conductor; and

the second delay circuit further comprises:

a second capacitor having a first electrode coupled to both the control electrode of the second current shunting device ant the first terminal of the second resistive device, the second capacitor having a second electrode coupled to the second power supply voltage conductor.

18. The circuit of claim **15** wherein the third power supply voltage conductor is further electrically connected to the first and second current shunting devices at a node between the first and second current shunting devices.

* * * * *

JS 44 (Rev. 12/07) (cand rev 1-16-08)

CIVIL COVER SHEET

ORIGINAL

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON PAGE TWO OF THE FORM.)

ADR

E-FILING

C08 00979 BZ

I. (a) PLAINTIFFS

MAXIM INTEGRATED PRODUCTS, INC.

DEFENDANTS

FREESCALE SEMICONDUCTOR, INC.

(b) County of Residence of First Listed Plaintiff (EXCEPT IN U.S. PLAINTIFF CASES)

County of Residence of First Listed Defendant Travis County, Texas (IN U.S. PLAINTIFF CASES ONLY)

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE LAND INVOLVED.

(c) Attorney's (Firm Name, Address, and Telephone Number)

Alan Blankenheimer, Esq., Laura Underwood-Muschamp, Esq., Jo Dale Carothers, Esq., HELLER EHRMAN LLP, 4350 La Jolla Village Drive, 7th Floor, San Diego, California 92122, Telephone: (858) 450-8400, Facsimile: (858) 450-8499

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff
- ☐ 2 U.S. Government Defendant
- ☐ 4 [redacted] (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant) (For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business In This State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business In Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. NATURE OF SUIT (Place an "X" in One Box Only)

CONTRACT
- 110 Insurance
- 120 Marine
- 130 Miller Act
- 140 Negotiable Instrument
- 150 Recovery of Overpayment & Enforcement of Judgment
- 151 Medicare Act
- 152 Recovery of Defaulted Student Loans (Excl. Veterans)
- 153 Recovery of Overpayment of Veteran's Benefits
- 160 Stockholders' Suits
- 190 Other Contract
- 195 Contract Product Liability
- 196 Franchise

REAL PROPERTY
- 210 Land Condemnation
- 220 Foreclosure
- 230 Rent Lease & Ejectment
- 240 Torts to Land
- 245 Tort Product Liability
- 290 All Other Real Property

TORTS

PERSONAL INJURY
- 310 Airplane
- 315 Airplane Product Liability
- 320 Assault, Libel & Slander
- 330 Federal Employers' Liability
- 340 Marine
- 345 Marine Product Liability
- 350 Motor Vehicle
- 355 Motor Vehicle Product Liability
- 360 Other Personal Injury

PERSONAL INJURY
- 362 Personal Injury—Med. Malpractice
- 365 Personal Injury — Product Liability
- 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- 370 Other Fraud
- 371 Truth in Lending
- 380 Other Personal Property Damage
- 385 Property Damage Product Liability

CIVIL RIGHTS
- 441 Voting
- 442 Employment
- 443 Housing/ Accommodations
- 444 Welfare
- 445 Amer. w/Disabilities - Employment
- 446 Amer. w/Disabilities – Other
- 440 Other Civil Rights

PRISONER PETITIONS
- 510 Motions to Vacate Sentence

Habeas Corpus:
- 530 General
- 535 Death Penalty
- 540 Mandamus & Other
- 550 Civil Rights
- 555 Prison Condition

FORFEITURE/PENALTY
- 610 Agriculture
- 620 Other Food & Drug
- 625 Drug Related Seizure of Property 21 USC 881
- 630 Liquor Laws
- 640 R.R. & Truck
- 650 Airline Regs.
- 660 Occupational Safety/Health
- 690 Other

LABOR
- 710 Fair Labor Standards Act
- 720 Labor/Mgmt. Relations
- 730 Labor/Mgmt.Reporting & Disclosure Act
- 740 Railway Labor Act
- 790 Other Labor Litigation
- 791 Empl. Ret. Inc Security Act

IMMIGRATION
- 462 Naturalization Application
- 463 Habeas Corpus – Alien Detainee
- 465 Other Immigration Actions

BANKRUPTCY
- 422 Appeal 28 USC 158
- 423 Withdrawal 28 USC 157

PROPERTY RIGHTS
- 820 Copyrights
- [redacted]

SOCIAL SECURITY
- 861 HIA (1395ff)
- 862 Black Lung (923)
- 863 DIWC/DIWW (405(g))
- 864 SSID Title XVI
- 865 RSI (405(g))

FEDERAL TAX SUITS
- 870 Taxes (U.S. Plaintiff or Defendant)
- 871 IRS—Third Party 26 USC 7609

OTHER STATUTES
- 400 State Reapportionment
- 410 Antitrust
- 430 Banks and Banking
- 450 Commerce
- 460 Deportation
- 470 Racketeer Influenced and Corrupt Organizations
- 480 Consumer Credit
- 490 Cable/Sat TV
- 810 Selective Service
- 850 Securities/Commodities/ Exchange
- 875 Customer Challenge 12 USC 3410
- 890 Other Statutory Actions
- 891 Agricultural Acts
- 892 Economic Stabilization Act
- 893 Environmental Matters
- 894 Energy Allocation Act
- 895 Freedom of Information Act
- 900 Appeal of Fee Determination Under Equal Access to Justice
- 950 Constitutionality of State Statutes

V. ORIGIN (Place an "X" in One Box Only)

[redacted] ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing **(Do not cite jurisdictional statutes unless diversity):**

[redacted] 2201 and 2202; 35 U.S.C. §1 et seq.

Brief description of cause:

Declaratory Judgment Action regarding U.S. Patents

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A **CLASS ACTION** UNDER F.R.C.P. 23

DEMAND $

CHECK YES only if demanded in complaint

JURY [redacted] ☒ Yes ☐ No

VIII. RELATED CASE(S) IF ANY

PLEASE REFER TO CIVIL L.R. 3-12 CONCERNING REQUIREMENT TO FILE "NOTICE OF RELATED CASE".

IX. DIVISIONAL ASSIGNMENT (CIVIL L.R. 3-2)

(PLACE AND "X" IN ONE BOX ONLY)

☐ SAN FRANCISCO/OAKLAND [redacted]

DATE

February 15, 2008

SIGNATURE OF ATTORNEY OF RECORD

Alan Blankenheimer /BZ

JS 44 Reverse (Rev. 12/07)

INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS 44

Authority For Civil Cover Sheet

The JS 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

I. **(a) Plaintiffs-Defendants.** Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.

(b) County of Residence. For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)

(c) Attorneys. Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)".

II. **Jurisdiction.** The basis of jurisdiction is set forth under Rule 8(a), F.R.C.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.

United States plaintiff. (1) Jurisdiction based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here.

United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.

Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.

Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; federal question actions take precedence over diversity cases.)

III. **Residence (citizenship) of Principal Parties.** This section of the JS 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.

IV. **Nature of Suit.** Place an "X" in the appropriate box. If the nature of suit cannot be determined, be sure the cause of action, in Section VI below, is sufficient to enable the deputy clerk or the statistical clerks in the Administrative Office to determine the nature of suit. If the cause fits more than one nature of suit, select the most definitive.

V. **Origin.** Place an "X" in one of the seven boxes.

Original Proceedings. (1) Cases which originate in the United States district courts.

Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C., Section 1441. When the petition for removal is granted, check this box.

Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.

Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.

Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.

Multidistrict Litigation. (6) Check this box when a multidistrict case is transferred into the district under authority of Title 28 U.S.C. Section 1407. When this box is checked, do not check (5) above.

Appeal to District Judge from Magistrate Judgment. (7) Check this box for an appeal from a magistrate judge's decision.

VI. **Cause of Action.** Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC 553
Brief Description: Unauthorized reception of cable service

VII. **Requested in Complaint.** Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.

Demand. In this space enter the dollar amount (in thousands of dollars) being demanded or indicate other demand such as a preliminary injunction.

Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.

VIII. **Related Cases.** This section of the JS 44 is used to reference related pending cases if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

Date and Attorney Signature. Date and sign the civil cover sheet.

ORIGINAL

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

MAXIM INTEGRATED PRODUCTS, INC.,

Plaintiff,

v.

FREESCALE SEMICONDUCTOR, INC.,

Defendant.

Case No. C 08 00979 BZ

COMPLAINT FOR DECLARATORY JUDGMENT AND DEMAND FOR JURY TRIAL

Plaintiff Maxim Integrated Products, Inc. ("Maxim"), for its Complaint against Defendant Freescale Semiconductor, Inc. ("Freescale"), avers as follows:

PARTIES

1. Plaintiff Maxim is a corporation organized and existing under the laws of the state of Delaware, with its principal place of business at 120 San Gabriel Drive, Sunnyvale, California 94086.

2. On information and belief, Defendant Freescale is a corporation organized and existing under the laws of Delaware, with its principal place of business at 6501

William Cannon Drive West, Austin, Texas 78735, which does business in this District and elsewhere in the State of California.

JURISDICTION AND VENUE

3. This action seeks a declaratory judgment under the Declaratory Judgment Act, 28 U.S.C. §§2201 and 2202. It presents an actual case or controversy under Article III of the United States Constitution and serves a useful purpose in clarifying and settling the legal rights at issue.

4. Freescale claims to own the following patents (collectively, "the Freescale patents"):

U.S. Patent No. 4,951,005 ("the '005 patent") entitled "Phase locked loop with reduced frequency/phase lock time," a true and correct copy of which is attached as Exhibit A,

U.S. Patent No. 5,008,615 ("the '615 patent") entitled "Means and method for testing integrated circuits attached to a leadframe," a true and correct copy of which is attached as Exhibit B,

U.S. Patent No. 5,081,454 ("the '454 patent") entitled "Automatic A/D converter operation using programmable sample time," a true and correct copy of which is attached as Exhibit C,

U.S. Patent No. 5,089,722 ("the '722 patent") entitled "High speed output buffer circuit with overlap current control," a true and correct copy of which is attached as Exhibit D,

U.S. Patent No. 5,105,250 ("the '250 patent") entitled "Heterojunction bipolar transistor with a thin silicon emitter," a true and correct copy of which is attached as Exhibit E,

U.S. Patent No. 5,172,214 ("the '214 patent") entitled "Leadless semiconductor device and method for making the same," a true and correct copy of which is attached as Exhibit F,

U.S. Patent No. 5,195,655 ("the '655 patent") entitled "Integrated fluid dispense

apparatus to reduce contamination," a true and correct copy of which is attached as Exhibit G,

U.S. Patent No. 5,200,362 ("the '362 patent") entitled "Method of attaching conductive traces to an encapsulated semiconductor die using a removable transfer film," a true and correct copy of which is attached as Exhibit H,

U.S. Patent No. 5,434,739 ("the '739 patent") entitled "Reverse battery protection circuit," a true and correct copy of which is attached as Exhibit I,

U.S. Patent No. 5,476,816 ("the '816 patent") entitled "Process for etching an insulating layer after a metal etching step," a true and correct copy of which is attached as Exhibit J,

U.S. Patent No. 5,593,538 ("the '538 patent") entitled "Method for etching a dielectric layer on a semiconductor," a true and correct copy of which is attached as Exhibit K,

U.S. Patent No. 5,776,798 ("the '798 patent") entitled Semiconductor package and method thereof," a true and correct copy of which is attached as Exhibit L,

U.S. Patent No. 5,124,632 ("the '632 patent") entitled "Low-voltage precision current generator," a true and correct copy of which is attached as Exhibit M,

U.S. Patent No. 5,861,347 ("the '347 patent") entitled "Method for forming a high voltage gate dielectric for use in integrated circuit," a true and correct copy of which is attached as Exhibit N, and

U.S. Patent No. 5,946,177 ("the '177 patent") entitled "Circuit for electrostatic discharge protection," a true and correct copy of which is attached as Exhibit O.

5. Maxim seeks a judgment against Freescale that the accused Maxim products and processes have not infringed and do not infringe the asserted claims of the Freescale patents and/or that these claims are invalid and/or unenforceable.

6. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a) because the action arises under the patent laws of the United States, 35

U.S.C. §1 et seq.

7. Venue in this district is proper pursuant to 28 U.S.C. §§ 1391(b) and (c).

INTRADISTRICT ASSIGNMENT

8. This action is an intellectual property case and pursuant to Civil L.R. 3.2(c), it should be assigned on a districtwide basis.

GENERAL ALLEGATIONS

9. Maxim manufactures and sells various semiconductor devices or integrated circuits.

10. On November 16, 2005, Freescale provided a book of patent claim charts to Maxim alleging that Maxim and/or Maxim devices infringe various patents, including the '615 patent, the '454 patent, the '722 patent, the '250 patent, the '632 patent, the '655 patent, the '739 patent, the '816 patent, the '798 patent, the '347 patent, the '177 patent ("the first set of Freescale patents").

11. In a subsequent letter dated July 14, 2006, Freescale specifically stated its claim charts previously provided for the first set of Freescale patents "provide notice to Maxim regarding infringement of [the first set of] Freescale patents by Maxim products." With this letter, Freescale also provided ten new claim charts, including charts for the '214 patent, the '538 patent, the '362 patent, and the '005 patent ("the second set of Freescale patents"), which Freescale alleged "provide notice of [] new patents to Maxim, and identify new Maxim products."

12. Freescale asserts that Maxim infringes the Freescale patents and needs a license to these patents, but Maxim disagrees. Maxim and Freescale met via conference call on August 8, 2007, November 30, 2007, and January 7, 2008, and in person on February 15, 2008, in an attempt to resolve the dispute.

13. Maxim and Freescale have been unable to reach any agreement with respect to Freescale's patent infringement allegations. Those discussions are now at an impasse.

14. Maxim is not liable for infringing any asserted claim of the Freescale patents because each such claim is invalid, the accused Maxim products and processes have not

infringed any such valid claim, and/or the asserted claims are unenforceable.

15. Accordingly, there is an actual, substantial and continuing justiciable controversy between Maxim and Freescale regarding the validity and enforceability of the Freescale patents and regarding alleged infringement of the Freescale patents by Maxim or by use of Maxim's products and processes.

FIRST CLAIM FOR RELIEF

Declaratory Relief — the '005 Patent

16. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-15 of the Complaint.

17. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '005 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

SECOND CLAIM FOR RELIEF

Declaratory Relief — the '615 Patent

18. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-17 of the Complaint.

19. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '615 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

THIRD CLAIM FOR RELIEF

Declaratory Relief — the '454 Patent

20. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-19 of the Complaint.

21. Maxim seeks and is entitled to a declaration that its accused products and/or

processes do not directly or indirectly infringe any asserted claim of the '454 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

FOURTH CLAIM FOR RELIEF

Declaratory Relief — the '722 Patent

22. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-21 of the Complaint.

23. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '722 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

FIFTH CLAIM FOR RELIEF

Declaratory Relief — the '250 Patent

24. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-23 of the Complaint.

25. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '250 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

SIXTH CLAIM FOR RELIEF

Declaratory Relief — the '214 Patent

26. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-25 of the Complaint.

27. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '214 patent and/or

that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

SEVENTH CLAIM FOR RELIEF

Declaratory Relief — the '655 Patent

28. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-27 of the Complaint.

29. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '655 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

EIGHTH CLAIM FOR RELIEF

Declaratory Relief — the '362 Patent

30. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-29 of the Complaint.

31. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '362 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

NINTH CLAIM FOR RELIEF

Declaratory Relief — the '739 Patent

32. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-31 of the Complaint.

33. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '739 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the

conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

TENTH CLAIM FOR RELIEF

Declaratory Relief — the '816 Patent

34. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-33 of the Complaint.

35. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '816 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

ELEVENTH CLAIM FOR RELIEF

Declaratory Relief — the '538 Patent

36. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-35 of the Complaint.

37. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '538 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

TWELFTH CLAIM FOR RELIEF

Declaratory Relief — the '798 Patent

38. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-37 of the Complaint.

39. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '798 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United

States Code.

THIRTEENTH CLAIM FOR RELIEF

Declaratory Relief — the '632 Patent

40. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-39 of the Complaint.

41. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '632 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

FOURTEENTH CLAIM FOR RELIEF

Declaratory Relief — the '347 Patent

42. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-41 of the Complaint.

43. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '347 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

FIFTEENTH CLAIM FOR RELIEF

Declaratory Relief — the '177 Patent

44. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-43 of the Complaint.

45. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '177 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

PRAYER FOR RELIEF

Wherefore, Maxim prays for relief as follows:

1. On Maxim's First through Fifteenth Claims for Relief:

(a) For a declaratory judgment that Maxim's accused products and processes do not infringe, contributorily infringe or induce infringement of, and have never infringed, contributorily infringed or induced infringement of, one or more claims of the Freescale patents;

(b) For a declaratory judgment that one or more claims of the Freescale Patents are invalid and/or that one or more of the Freescale Patents are unenforceable;

(c) For the Court to declare this to be an exceptional case within the meaning of 35 U.S.C. § 285, entitling Maxim to an award of its reasonable attorneys' fees in this action;

(d) For an award to Maxim of all costs and expenses of this action; and

(d) For such other and further relief as the Court may deem just and proper.

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February 15, 2008

Respectfully submitted,

HELLER EHRMAN LLP

By _____
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LAURA E. UNDERWOOD-MUSCHAMP (BAR NO. 228717)
JO DALE CAROTHERS (BAR NO. 228703)

Attorneys for Plaintiff
MAXIM INTEGRATED PRODUCTS, INC.

DEMAND FOR JURY TRIAL

Plaintiff Maxim demands a jury trial on all issues triable of right by jury.

February 15, 2008

Respectfully submitted,

HELLER EHRMAN LLP

By _____
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